Substrate Coupling: Modeling and Mitigation Techniques

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ECE 465: Performance Issues in VLSI IC Design

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Outline

- Substrate coupling mechanism
- Modeling techniques
- Mitigation techniques
- Conclusions
- Future directions

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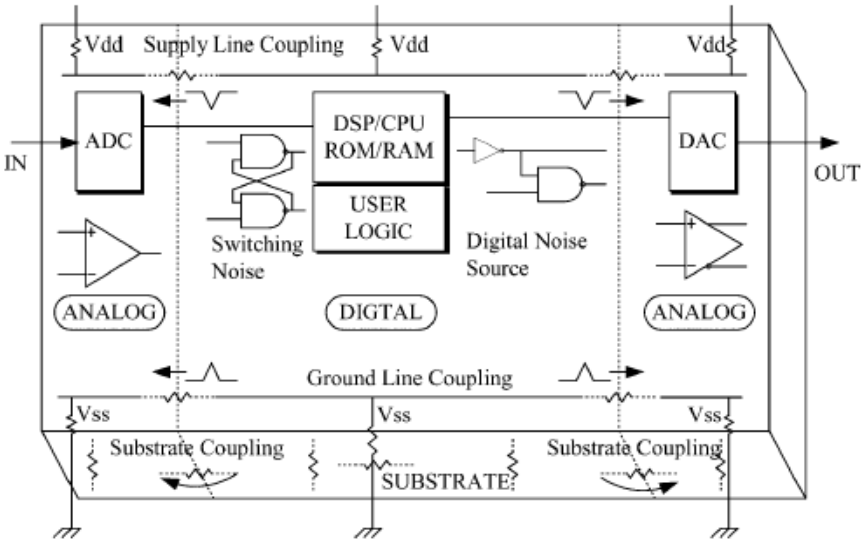
What is Substrate Coupling?

- Substrate coupling
  - Coupling of digital switching noise to analog/RF circuits through substrate
- Why it is undesired?
  - Causes voltage fluctuations
  - Signal leakage causes power loss
  - Degrades performance of sensitive amplifiers, oscillators#



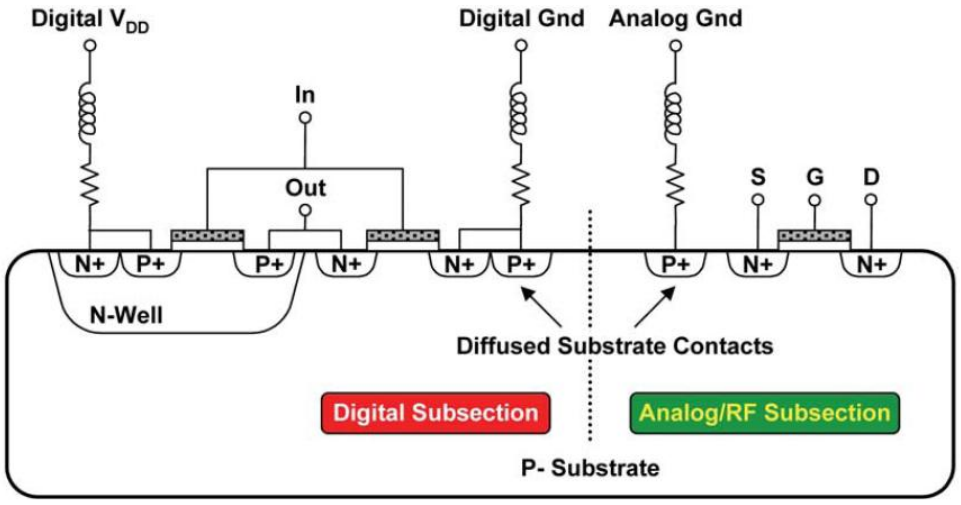
Substrate coupling noise in mixed-signal SoC

Afzali-Kusha *et al.*, "**Substrate Noise Coupling in SoC Design: Modeling, Avoidance, and Validation**," *in Proceedings of the IEEE*, 2006.

B. R. Stanisic *et al*., "**Addressing substrate coupling in mixed-mode ICs: Simulation and power distribution systems** ,", *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 226–238, Mar.1994.

Impact of Substrate Coupling on Circuit Performance

- Operating conditions
  - Threshold voltage modulation
  - Bias current
- Degradations
  - Gain, bandwidth
  - Jitter, SNR
- Failures
  - Latchup



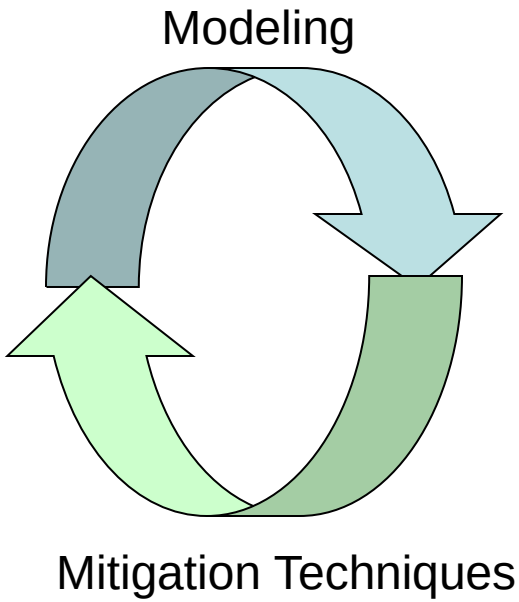
*Noise coupling from switching portion of an IC

Ranjit Gharpurey and Edoardo Charbon, "**Substrate Coupling: Modeling, Simulation and Design Perspectives**," *in Proceedings of the International Symposium on Quality Electronic Design*, pp. 283-290, 2004.

* Afzali-Kusha *et al.*, "**Substrate Noise Coupling in SoC Design: Modeling, Avoidance, and Validation**," *in Proceedings of the IEEE*, 2006.

Substrate Coupling Methodologies

- Two aspects of substrate coupling research
  - Modeling the substrate coupling
    - Substrate extraction
    - Parasitics extraction
  - Techniques to mitigate the coupling noise
    - Physical design techniques
    - Circuit based technique
- Accurate modeling enables better mitigation techniques



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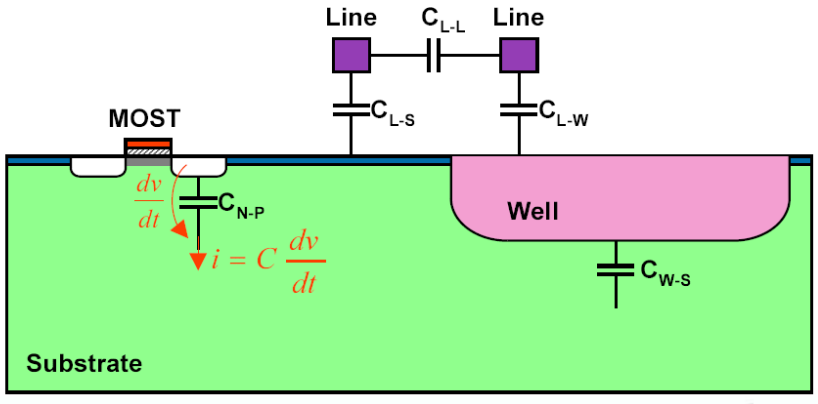
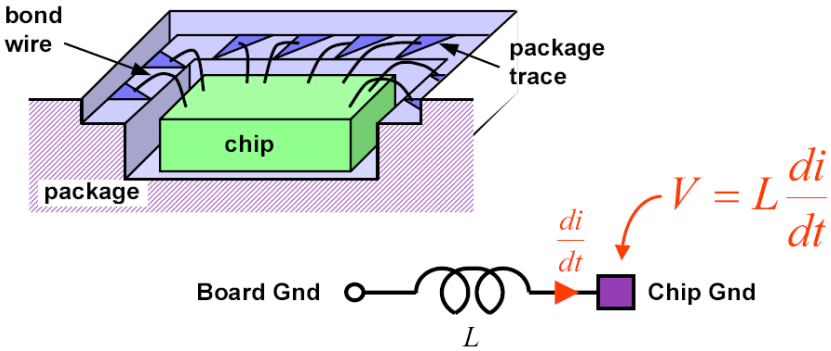
Substrate Coupling at Various Level

- Impact ionization
  - **At device level**
  - Substrate current injection
- Capacitive coupling (C*dv/dt)
  - **At circuit level**
  - Due to junction capacitance
  - Interconnect capacitance to substrate
- Inductive (L*di/dt) and resistive (i*R) noise
  - **At chip level**
  - Large di/dt on power supply at high frequency
  - Resistive drop at low frequency

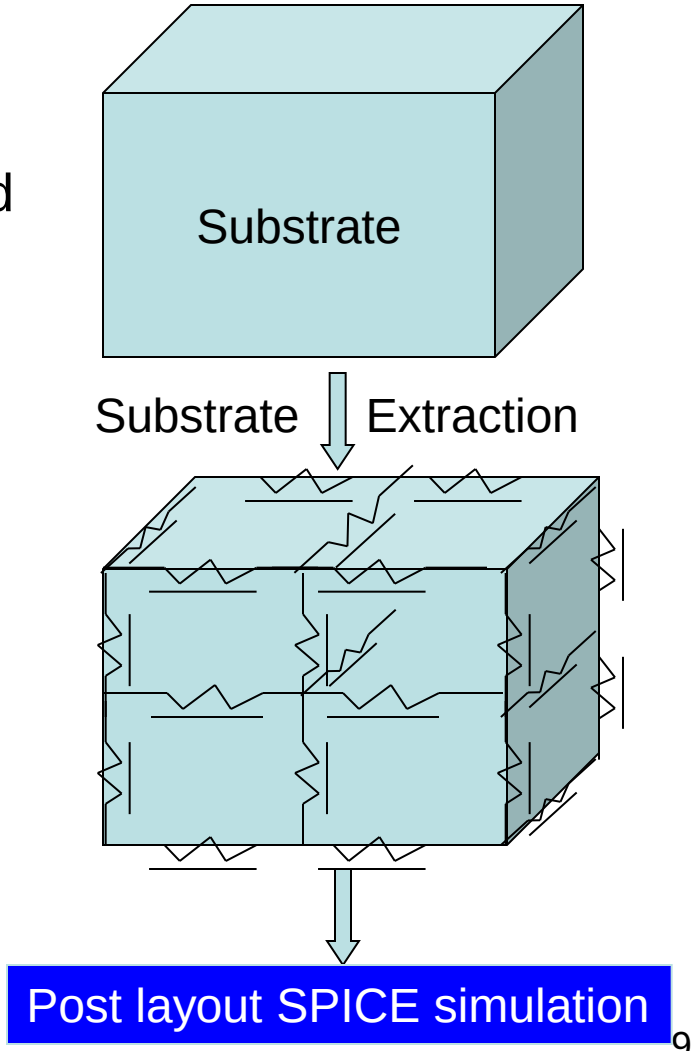




R. Gharpurey and R. G. Meyer, "**Modeling and Analysis of Substrate Coupling in ICs**," *in Proceedings of the IEEE CICC*, pp. 125-128, May 1995.

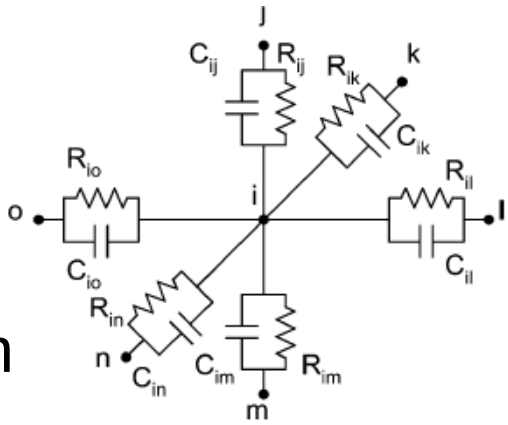
Substrate Extraction

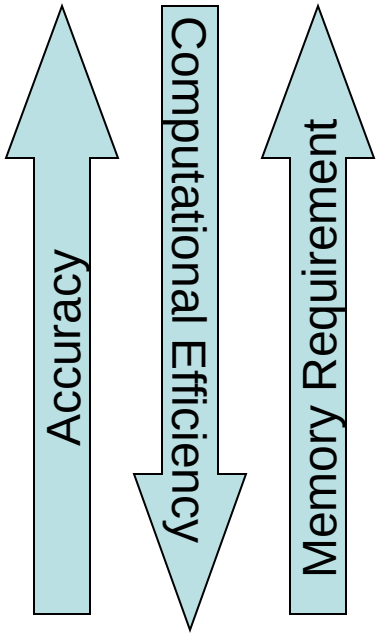
- Extraction
  - Process by which an RC equivalent circuit of the substrate is determined
- Accomplished by solving electromagnetic differential equations
- Extracted RC mesh is simulated using SPICE
- RC values are incorporated
  - Post layout SPICE simulation



Modeling Coupling to Substrate

- Integral-equation technique
  - Distributed RC mesh
- Solution techniques to model RC mesh
  - Finite elements (FEM)
    - Exact solution using Poisson and continuity equations
  - Finite differences (FDM)
    - Simple RC model applied on 3D Mesh
  - Boundary element (BEM)
    - Only port-to-port relationship needs to be modeled

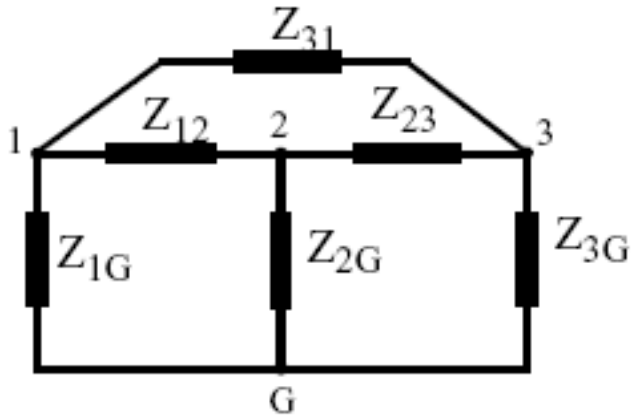




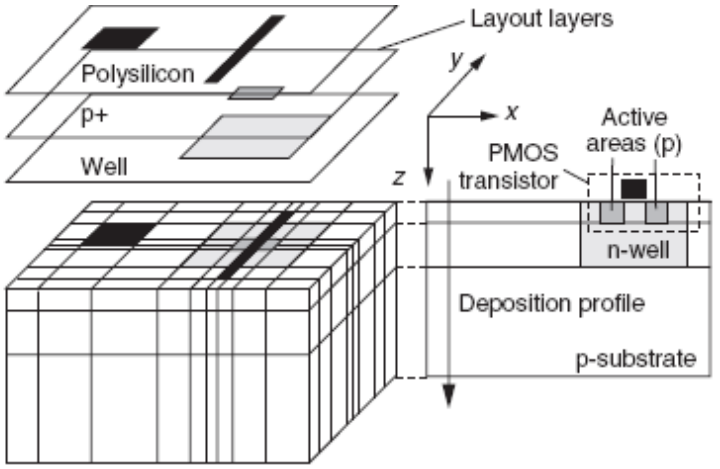
Silva, J. M. and Silveira, L. M., "**Substrate model extraction using finite differences and parallel multigrid**", *Integr. VLSI J.* 40, 4 (Jul. 2007), 447-460.

Small Circuit Extraction

- Lumped models
  - Advantages
    - Accuracy ↑
  - Drawbacks
    - Extraction/ Simulation time ↑



- Distributed models
  - Appropriate formulation of substrate electromagnetic interactions
  - Rely on numerical methods
    - MEDICI, PISCES



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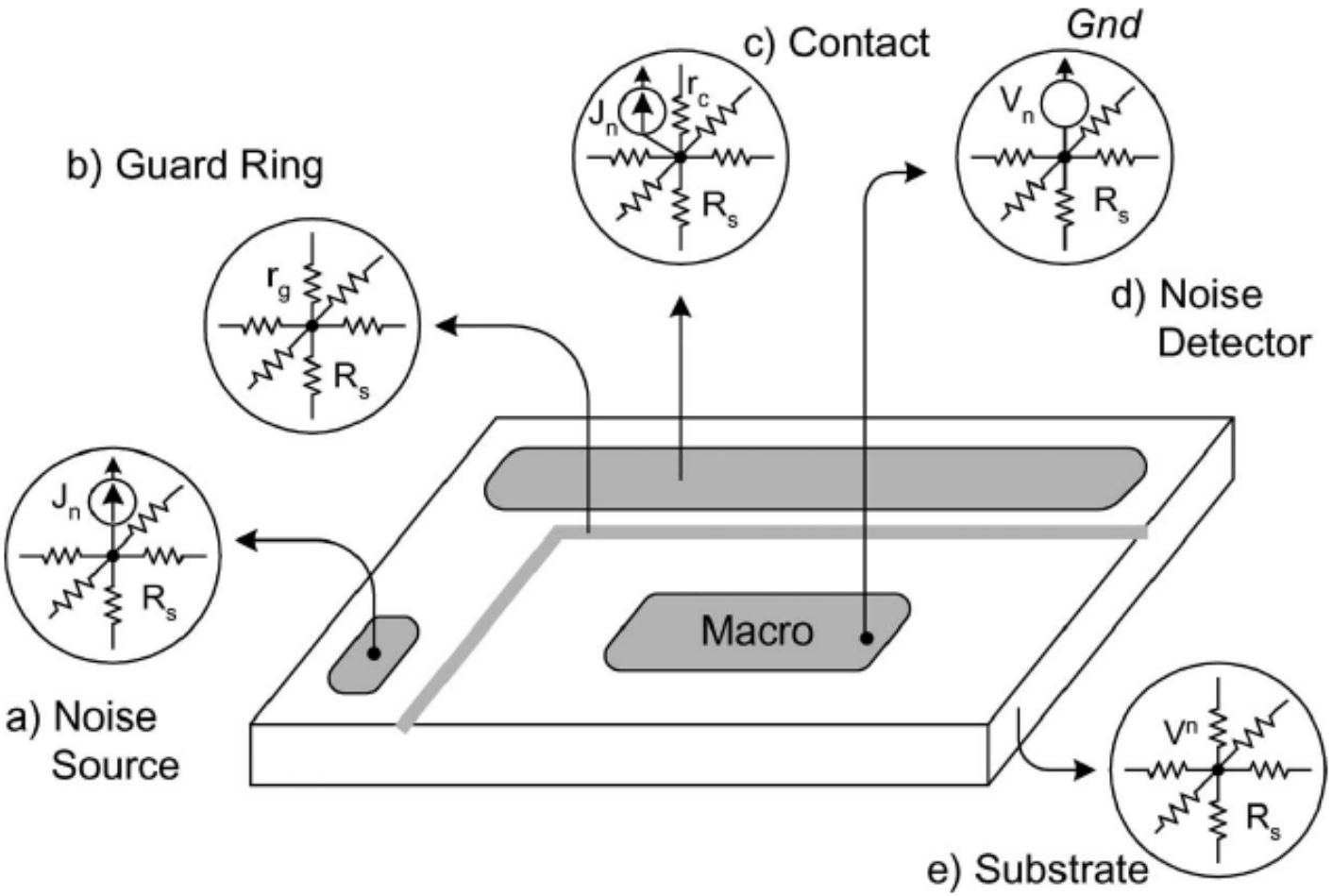
Substrate Resistive Macro-model



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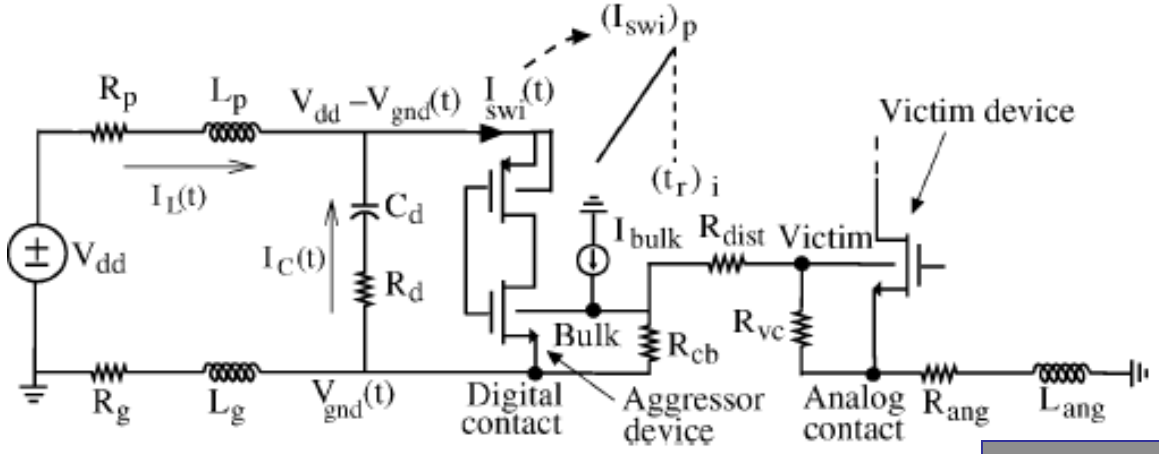
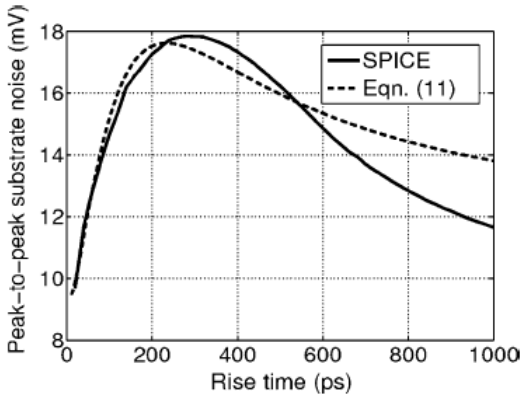
Analysis using Macro-models

- Macro-model presented here helps in early stage of design process
  - Evaluates the dominant substrate coupling mechanism
  - Exhibits a maximum error of ~18.4%; Mainly due to
    - Approximation of noise as a ramp function
    - Feedback effect of the nonlinear devices are ignored in the model





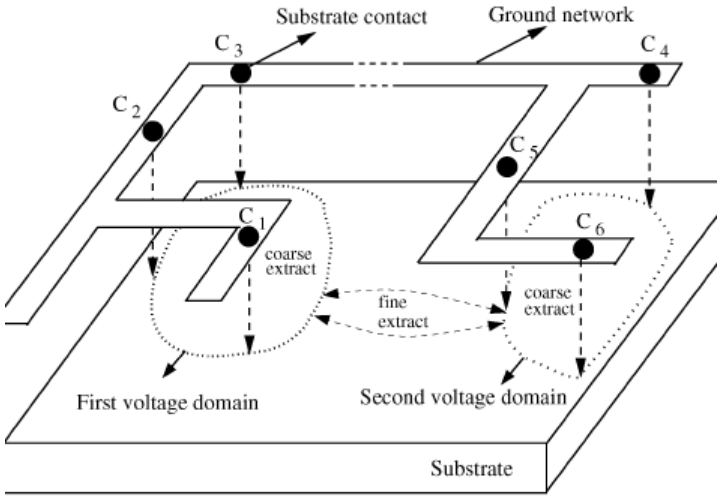
$$(V_{s-total})_{pp} \approx (V_{s-gnd})_{pp} + (V_{s-bulk})_p.$$

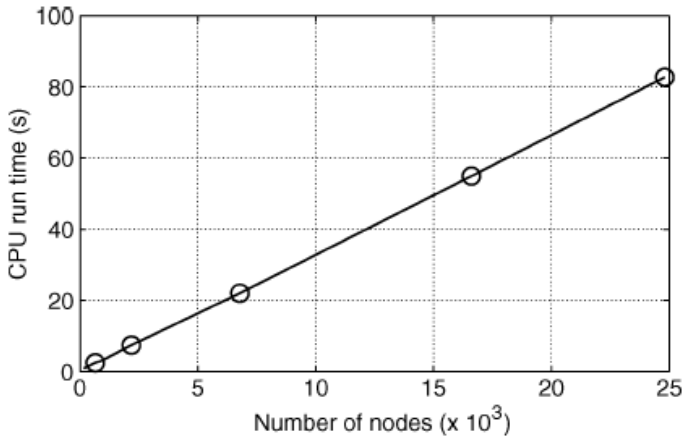
$$(V_{s-bulk})_p \approx (I_{bulk})_p \frac{R_{cb}}{R_{cb} + R_{dist} + R_{vc}} \times \left(R_{ang} + R_{vc} + \frac{L_{ang}}{t_r} \right).$$

E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, " **Identification of Dominant Noise Source and Parameter Sensitivity for Substrate Coupling**," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 10, pp. 1559-1564, October 2009.

Large Scale Mixed-Signal Circuits

- Transistor level simulation is not feasible for large-scale circuits
  - Nonlinear nature of the device models
  - Computationally inefficient
- Voltage domains on the substrate
  - Coarse extraction in each domain to reduce the computational complexity
  - Followed by a fine extraction of those domains where the dominant current flow occurs
  - Linear complexity of algorithm





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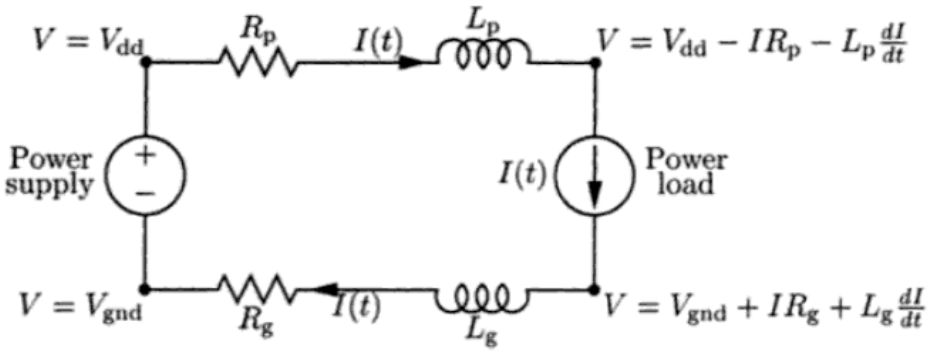
Physical Design Techniques

- Power network design techniques
  - At high frequency inductance noise dominates
  - Special care to minimize di/dt

$$V_{drop} = Ri + L\frac{di}{dt}$$

- Architectural solutions to di/dt
  - RAZOR flip flops*
  - Traditional sensor based control#

- Mainly to solve low or mid range inductive noise

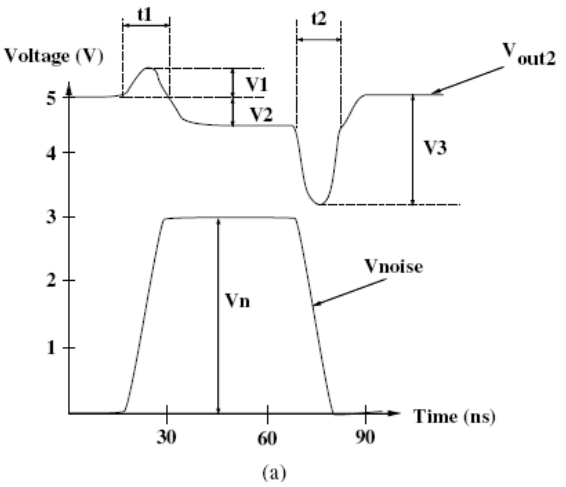


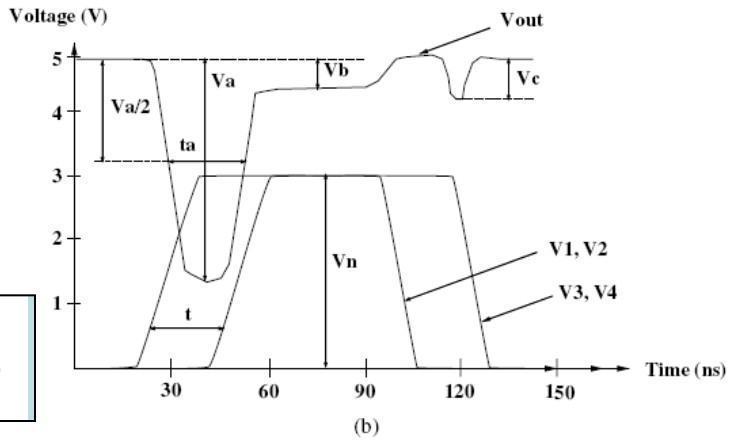
- High frequency inductive noise
  - No architectural solution exist
  - Only circuit based solutions
    - Use of decoupling capacitors

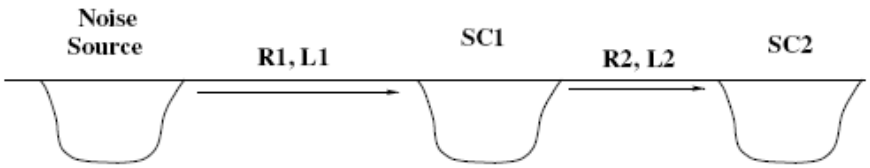
M. El-Moursy and E. Friedman, ***On-Chip Inductive Interconnect Design Methodologies***, VDM Verlag Dr. Muller Aktiengesellschaft & Company, 2009.

Physical Design Techniques - 2

- Layout techniques to improve the uniformity
  - A compact layout is beneficial to improve the uniformity of the substrate noise received by the different transistors
- Placement of substrate contact





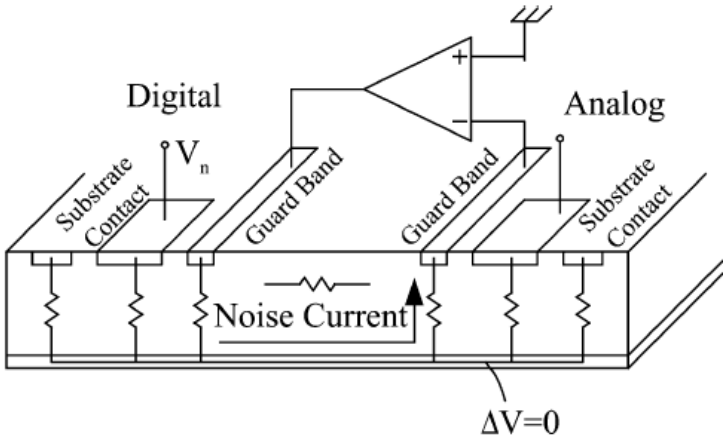


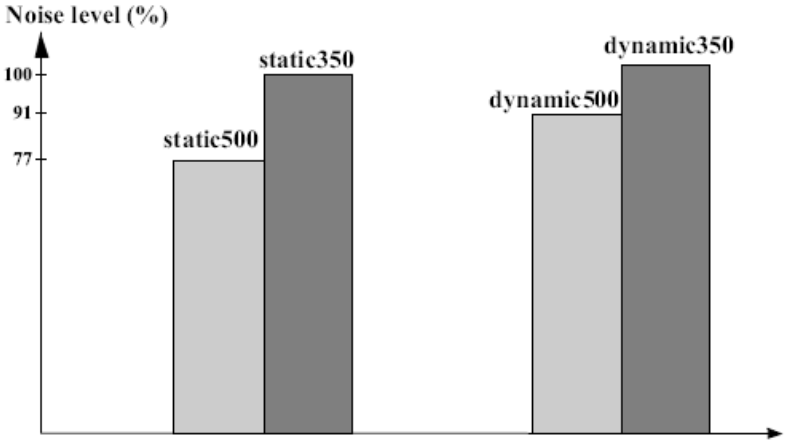
$$\frac{R_1}{R_2} \ll 1.$$

Secareanu, R. M., Warner, S., Seabridge, S., Burke, C., Watrobski, T. E., Morton, C., Staub, W., Tellier, T., and Friedman, E. G., "**Placement of Substrate Contacts to Minimize Substrate Noise in Mixed-Signal Integrated Circuits**", *Analog Integr. Circuits Signal Process.* 28, 3 (Sep. 2001), 253-264.

Circuit Design Techniques

- Active guard band filters
- Active cancellation circuits
  - Differential ended analog circuits
  - Repeater insertion for improved noise immunity
- Register positioning and orientation to minimize noise
  - Static register as oppose to dynamic registers
- Choice of logic family also plays an important role in noise mitigation

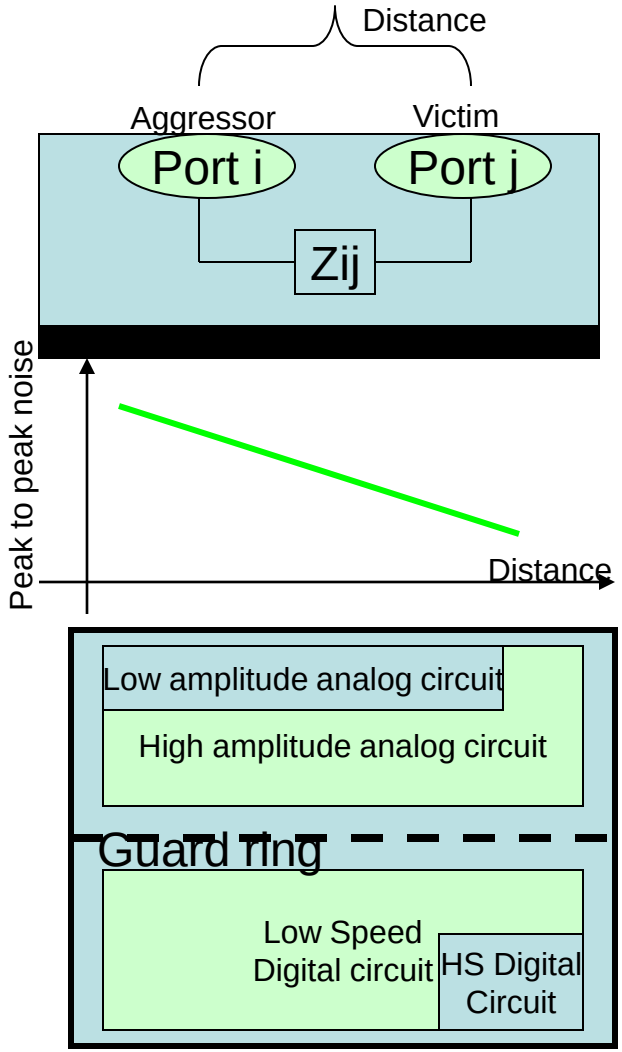




Secareanu, R. M. et al., "**Substrate coupling in digital circuits in mixed-signal smart-power systems**", *IEEE Trans. VLSI Systems.,* 2004.

Isolation Techniques

- Separate digital and analog supply
  - Switching noise is not coupled from one domain to other domain
- Distance isolation
  - Reduces the amplitude of noise
- Isolation of noise source
  - Ensures that noise is not injected
- Careful floorplanning
  - Place sensitive digital and analog blocks ***furthest*** from each other



R.M. Secareanu, S. Warner, S. Seabridge, C. Burke, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "**Physical design to improve the noise immunity of digital circuits in a mixed-signal smart power system**," *in Proc. IEEE Int. Symp. Circuits Systems*, May 2000, pp. 4.277-4.280.

Guidelines to Mitigate Noise

- Separate analog and digital power lines
- Physically separate the noise generating circuit and noise sensitive circuit
- Guard ring with good substrate contacts placed between digital and analog circuits
  - Connect the rings to external “quiet” ground
- Differential ended analog circuits
  - Robust and have good noise rejection capability
    - Good CMRR and PSRR

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Conclusions

- Switching noise of digital block affects sensitive analog/RF blocks through substrate coupling
- Modeling the substrate coupling with high accuracy for large chips is a daunting and resource consuming task
- Multiple techniques – physical and circuit based – should be used to mitigate substrate coupling noise
- Scaling of feature size and supply voltage would exacerbate the problem of the substrate coupling noise

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Future Directions

- Hard problems and open challenges
  - Related with modeling of large circuits
    - Computational complexity
    - Memory requirement
  - CAD tools and EDA flow
    - Integration of accurate substrate models into existing CAD flow

"All models are wrong, some are useful"
-- George E. P. Box

So another never-ending task for any research field is to
"Keep devising new models and macro-models"

References

- R. Gharpurey and R. G. Meyer, "**Modeling and Analysis of Substrate Coupling in ICs**," *in Proceedings of the IEEE CICC*, pp. 125-128, May 1995.
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- M. Nagata, T. Morie, and A. Iwata, "**Modeling substrate noise generation in CMOS digital integrated circuits**," *in Proceedings of the IEEE 2002 Custom Integrated Circuits Conference*, pp.501–504, May 2002.
- Afzali-Kusha *et al.*, "**Substrate Noise Coupling in SoC Design: Modeling, Avoidance, and Validation**,**"** *in Proceedings of the IEEE*, 2006.
- B. R. Stanisic *et al*., "**Addressing substrate coupling in mixed-mode ICs: Simulation and power distribution systems"**, *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 226–238, Mar.1994.
- Secareanu, R. M. et al., "**Substrate coupling in digital circuits in mixed-signal smart-power systems**", *IEEE Trans. VLSI Systems.,* 2004.
- E. Salman, R. Jakushokas, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, " **Methodology For Efficient Substrate Noise Analysis in Large Scale Mixed-Signal Circuits**," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 10, pp. 1405-1418, October 2009.
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- M. El-Moursy and E. Friedman, ***On-Chip Inductive Interconnect Design Methodologies***, VDM Verlag Dr. Muller Aktiengesellschaft & Company, 2009.

References (Cont …)

- Crovetti, P. S. and Fiori, F. L., "**Efficient BEM-based substrate network extraction in silicon SoCs**", *Microelectron. J.* 39, 12 (Dec. 2008), 1774-1784.
- Silva, J. M. and Silveira, L. M., "**Substrate model extraction using finite differences and parallel multigrid**", *Integr. VLSI J.* 40, 4 (Jul. 2007), 447-460.
- K. Makie-Fukuda, S. Maeda, T. Tsukada, and T. Matsuura, "**Substrate noise reduction using active guard band filters in mixed-signal integrated circuits**," *in Symposium on VLSI Circuits. Digest of Technical Papers*, 1995, pp. 33—34.
- Farivar, R., Kristiansson, S., Ingvarson, F., and Jeppson, "**Evaluation of using active circuitry for substrate noise suppression**," *In Proceedings of the 17th ACM Great Lakes Symposium on VLSI* , Stresa-Lago Maggiore, Italy, March 11 - 13, 2007.
- Secareanu, R. M., Kourtev, I. S., Becerra, J., Watrobski, T. E., Morton, C., Staub, W., Tellier, T., and Friedman, E. G., "**Noise Immunity of Digital Circuits in Mixed-Signal Smart Power Systems**," *In Proceedings of the Ninth Great Lakes Symposium on VLSI* (March 04 - 06, 1999).
- K. Makie-Fukuda and T. Tsukada, "**On-chip active guard band filters to suppress substrate coupling noise in mixed-signal integrated circuits**," *IEICE Trans. Electron*., vol.E83-C, no.10, pp.1663–1668, Oct. 2000.
- Secareanu, R. M., Warner, S., Seabridge, S., Burke, C., Watrobski, T. E., Morton, C., Staub, W., Tellier, T., and Friedman, E. G., "**Placement of Substrate Contacts to Minimize Substrate Noise in Mixed-Signal Integrated Circuits**", *Analog Integr. Circuits Signal Process.* 28, 3 (Sep. 2001), 253-264.
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