Imaging Solutions by Mercury Computer Systems

Presented By

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Mercury Computer Systems

- Boston based; designs and builds embedded multi computers
  - Loosely coupled NUMA computers, or
  - Tightly coupled clusters

- Typical Mercury’s embedded multi-computer
  - Dozens of CPUs
  - Packed into a space of foot or two

- Strong emphasizes on
  - Vector math
  - IO performance

- Today’s focus: High end (mainly medical) imaging solutions
High Density Processing

- Four MPC8640D dual-core processors
  - Each with two standard e600 processor cores
  - Can run up to 1.06 GHz

- Four 4x lanes of serial RapidIO with data rates at up to 3.125 GB/s

- Two 1000BASE-BX Gigabit Ethernet links (one for each MPC864xD device) to backplane

- PCI/PCI-X interface at up to 133 MHz on each site

- I2C interface to backplane

HCD6410 module can work as
- Standalone processing center, or
- as part of an embedded cluster for high-end digital signal processing

Ensemble 6000 series
Adjunct Processing in 3-D Image Reconstruction

- Accelerates Cone-Beam Reconstruction (CBR)
- Reduces CBR Reconstruction Time from 5-15 Minutes to 15 Seconds
- Adjunct processing engines are implemented using FPGAs
Imaging Solution of the Year: 2007

- Mercury’s Cell Acceleration Board (CAB)
  - Peak performance: 180 GFLOPS
  - Memory bandwidth: 25 GB/s

- Mercury’s MultiCore Plus™ SDK

- Mercury’s Trace Analysis Tool and Library (TATL)

- Capable of performing modern CT reconstruction more than 100 times faster than conventional microprocessors
Digital MRI Acquisition System

- Complete MRI solution
  - 5-25% improvement in scan quality

- Performance
  - 10 minutes as oppose to 25 minutes

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Digital MRI Receiver</th>
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<tbody>
<tr>
<td>Frequency range</td>
<td>5-400 MHz</td>
</tr>
<tr>
<td>Gain range</td>
<td>4-60 dB</td>
</tr>
<tr>
<td>Step size</td>
<td>1 dB</td>
</tr>
<tr>
<td>Noise figure</td>
<td>&lt; 4 dB</td>
</tr>
<tr>
<td>IP3</td>
<td>&gt; 44 dB</td>
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<tr>
<td>Data acquisition</td>
<td>16 bits</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>100 MHz</td>
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<tr>
<td>Dynamic range</td>
<td>24 bits by decimation</td>
</tr>
<tr>
<td>Data transfer</td>
<td>66 MHz x 64-bit PCI bus interface</td>
</tr>
<tr>
<td>Form factor</td>
<td>PCI short card</td>
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</tbody>
</table>
PixL Image Processing Algorithm Library

- Designed for RACE++ and RACE multicomputers from Mercury

- Includes ~130 image processing *hand-optimized* routines

- Accelerate integer mathematical operations by 8 to 16X over scalar operations

- Some well known image processing routines
  - Edge detection
  - General convolution
  - Histogram generation
  - Gradient detection
AMIRA: Scalable Visualization Framework

- Advanced visualization
- Data analysis
- Geometry reconstruction
On-chip Timing Uncertainty Measurements on IBM Microprocessors – SKKITER

R. Franch et.al.

Int’l Test Conference – 2007
Motivation

- Sources of timing uncertainty in microprocessor
  - PPL jitter
  - Clock distribution skew and jitter
  - Across chip device variations – PVT
  - Power supply noise – di/dt noise

- Conventional implementation of guard band
  - Summation all of the above
  - Highly conservative estimation of delay
  - Results into degraded performance

- IBM’s on-chip measurement macro (Skew + Jitter)
  - Placed into every core and nests
  - Read out in real time
Skitter Circuits: Operating Modes

- Edge capture and accumulate circuit

- Consecutive 1 or 0 represent edges
  - Location of edges changes when there is delay/ noise

- Doesn’t differentiate the sources
  - Gives the bottom-line effects of timing uncertainty from all the sources.

Changing location of edges $\rightarrow$ Variations in chip timings
Skitter with “Sticky” Register

- Records the worst-case excursions
  - A workload can be run overnight and the extremes of the short cycles or longest cycles can be recorded

Fig 2: Basic Skitter circuit with accumulation or “sticky” register
Single-sample vs Sticky Mode

Nominal Cycle:
10000000000000000000000000000000000000000100

Mid-cycle edge

Full Cycle Edge

Low Vdd Cycle
10000000000000000000000000000000010000000000000000010000000

Result: Identical to 8% shorter cycle

Result in sticky mode:
100000000000000000000000000000001110000000000000000000000111100

Fig 3: Edge movement due to low VDD (single-sample and sticky mode)

• “Hold” mode to read out the sticky register for a particular cycle
• Multiple Skitters → TO measure the clock skew
Experimental Results

- CELL BE Processor (1 PPC + 8 SPE)
  - Two Skitters; Placed several mm apart
  - Showed nearly identical results >> No timing uncertainty

- XBOX360 Processor (3-core PPC)
  - The chip was built with total 5 skitter circuits
  - Magnitude of timing uncertainty ~ 20%

- PPC970MP Processor (dual-core PPC)
  - Was built with 4 skitter circuits
  - Workload specific timing: ~ 10% uncertainties

- Power6 Processor (dual-core PPC)
  - Repetitive run of noise causing INS stream >> Oscilloscope
Conclusions

- Skitters has established as standard tool for testing a range of IBM chips
- Skitters give real-time combined effect of noise/timing uncertainty
- Lot of measurements are possible using skitters
  - Jitter, skew, worst-case violations
PicoServer: 3D Stacking to Implement Low Power CMP

ALPLOS – 2006

T. Kgil et al
Motivation

Targets Tier 1 server which exhibit High TLP
Tier 1 Server: Requirements

- Prime objectives are
  - High throughput
  - Low power

- How does 3D fit in?
  - DRAM are stacked on the top of CPU cores
  - *L2 cache is removed*; area is used for more cores
  - Additional cores allow to scale down the clock
  - Lower clock saves the power
  - TSVs provide high bandwidth
PicoServer: CMP Architecture

Top view

Side view
Key Improvements

- 3D stacking enables the following
  - High bandwidth
    - Between main memory (DRAM) and L1 caches
  - Modification in the memory hierarchy
    - Integration of large capacity on-chip DRAM
    - L2 cache is thrown away
  - Overall reduction in system power
    - Reduction in clock frequency due to additional cores
Block Diagrams

General purpose processor

PicoServer with 3D stacking
Results

- An 8-way PicoServer @ 500MHz in 90nm process technology
  - Network bandwidth: up to 1.1Gbps
  - Power Consumption: 3W

- These results are 2 to 3X better than a multicore architecture without 3D stacking technology.
Comparisons

- For same logic die area
  - Baseline: 8-CPU system with large on-chip L2
  - PicoServer: 12-CPU system with 3D stacking and no L2 cache
- Performance: PicoServer (14%)
- Power: PicoServer (55%)

- Compare to Pentium-4 like machines
  - Consumes 1/10 of power while same performance
Conclusions

- Trade off area for power and bandwidth
  - Probably a good trade-off
  - Also alleviates thermal issues

- No *real* innovation as per 3D is concerned
  - Plain vanilla 3D stacking
  - Approach would suffer as feature size shrinks
    - Break even: 3D via not comparable with local wires