Practicality of Single Event Effects Detection using thin-films: A Study

by

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Abstract

Single Event Effects are errors in electronic circuits caused by cosmic particles present in the natural environment. The result of a particle strike may corrupt the logical state at a target node or cause erroneous glitches. In most instances, the errors are random and non-destructive. The severity of these errors, however, cannot be discounted as exemplified by commercial instances [21, 22].

Particles from the outer space interact with the atmosphere to produce a cascade of secondary particles [2]. At ground level, neutrons dominate the particle composition [13]. However, alpha particles also significantly contribute to these errors. Since alpha particles can be easily shielded, only their on-chip sources are of importance [4].

At sea-level, the particle flux distribution of neutrons varies significantly across neutron energy [1, 13]. Two regions of this distribution are of particular interest; the neutrons at thermal energies (<1 eV), which account for almost 33% of all available neutrons, and high-energy (>1 MeV) neutrons (HEN) which constitute over 60% of all available neutrons. Since neutrons are electrically neutral, they do not cause ionization. Instead they are either absorbed or scattered by a target nucleus. The result of this is an ionizing particle. Ionizing particles, like alpha particles and heavy ions, create charge carriers in their traveling media by ionizing target atoms. If sufficient charge is collected in the active region, the logical state at that node could be altered [4].

Current techniques such as redundancy by duplication and radiation hardening are expensive [3]. For example, redundancy is needed to detect particle induced errors for random logic. Compared to circuit operations, particle impacts are extremely rare, making redundancy a very ineffective means of error detection. In thesis, the idea of directly detecting the incoming particle via a thin-film structure is explored.

Chapter 1

Introduction

Reliability and fault tolerance are amongst the essential criteria that govern circuit and system design. The success of Moore's law and advancements in fabrication process have placed innovation in circuit design far ahead of expectations. Figure 1.1 broadly defines the various layers that constitute modern machines. The success of a higher layer is heavily dependent on the integrity of the underlying structures. With growing ubiquity in computing, the need for a reliable system that consistently delivers the expected results is critical.

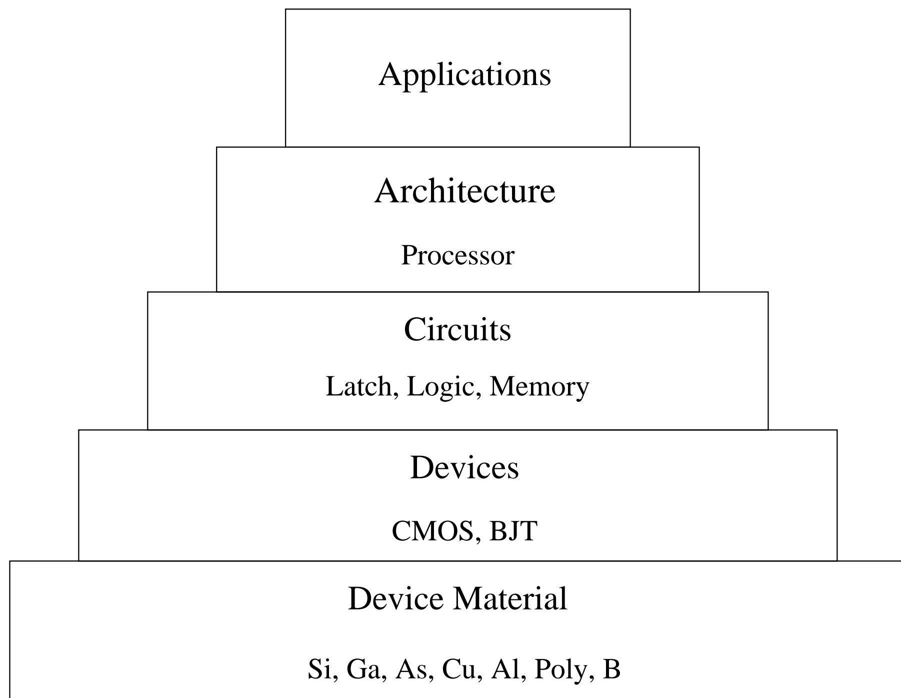


Figure 1.1: Layers in modern machine

Single event effects (SEE) are perturbations in electronic circuits caused by particles in the environment. The primary source of these particles is known to be cosmic rays, which upon interacting with the atmosphere, produce a cascade of secondary particles. The composition of these secondary particles vary with altitude and latitude. Since our interest is ground-based systems, we focus on particles at sea-level, where the primary particles considered are neutrons. Another source of errors is alpha particles from radioactive impurities present on-chip.

With shrinking transistor sizes and increasing integration densities, integrated circuits have become less tolerant to any form of noise. Errors can either be detected by the system or remain hidden. The latter is also known as silent data corruption (SDC). In SDC the user/system is unaware of the error occurrence and hence falsely accepts the integrity of the underlying functionality. Another way of classifying errors is based on permanence of the effect. Hard errors are those that have a permanent damage to the system, while soft errors are transient, and usually corrected by an overwrite or restart operation.

Based on the above description, soft errors that cannot be detected are deemed harmful to reliable computing. The term SEE is a broad category of various errors that can occur in a circuit. Figure 1.2 lists some of the errors.

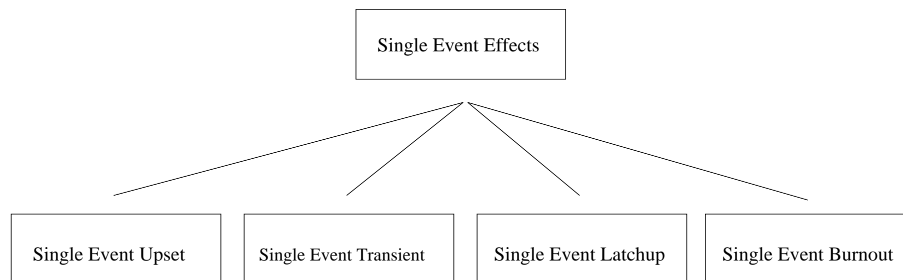


Figure 1.2: Different kinds of errors.

A particle strike may alter the logical state of a bistable element or setup a glitch through the circuit, the former is referred to as SEU while the latter is SET. SEL is the phenomenon where an imbalance in polarity, introduced by the external particle, turns on the parasitic bipolar transistors in bulk CMOS. This could lead to a short circuit and permanently damages the transistor. SEB is the class of errors where particle strikes produce sufficient energy to damage the circuit.

Various authors [3, 9] have presented a chronological summary of research milestones in this field. SEE in terrestrial circuits have been of interest since 1970s when alpha particle induced errors were noticed in DRAM circuits. Protons and neutrons were also reported to

cause errors. In 1990s, Baumann et al. [7] reported that thermal neutrons were the most significant cause for errors in integrated circuits. This was ascertained by the error reduction achieved by reducing the ^{10}B content on-chip. However, the error rates are expected to grow with diminishing feature size [7, 10].

Of considerable interest are the error trends in logic and memory. Memory operations are more predictable than logic. Further reliability techniques such as error correction apply more readily with memory circuits. At earlier technology generations which operated at a slower speed, the probability of an error being latched by the logic component was small, because the glitch introduced by a particle strike was much smaller compared to circuit propagation time. Error rates are usually expressed in FIT or Failures in Time. 1 FIT is an instance of an error in 10^9 device hours. In current technology, soft errors typically occur at a range of 100-1000kFIT/Mbit [7]. Approximately, this is equivalent to an error in every 400-40 days for every Mbit of data.

At these rates, fault tolerance is a desirable, if not necessary, feature of modern computing systems. However, error detection in random logic is challenging and generally requires full-blown duplication of circuitry, which incurs significant power and area overhead. Compared to activities inside a microprocessor, particle impact is extremely rare. As such, always-on redundancy to detect transient errors seems an exceedingly inefficient use of hardware resources and energy. In this thesis, we study the practicality of using thin film structures as a sensor to detect the incoming particles and trigger only on-demand redundancy to provide fault tolerance. The rest of the thesis is organized into the following chapters. Chapter 2 analyzes the particle composition at sea-level. Chapter 3 is a discussion on the passage of particles through matter. Chapter 4 presents the data on error analysis and trends with a brief overview of the effects of scaling. Chapter 5 presents the idea of detecting errors using thin films. Finally, a summary of the key idea is presented.

Chapter 2

Analysis of Terrestrial Particle Flux

Various phenomena in deep space are responsible for the transport of high energy (1-10 GeV) particles. The Sun, with its proximity to earth, is a major source of these particles. Some of these outer space particles interact with the earth's atmosphere and generate a completely new set of resultant particles. The composition of the generated particles change as they continue to interact with the atmosphere, thus producing a particle cascade. The particle flux at any point is a function of both latitude and altitude [2].

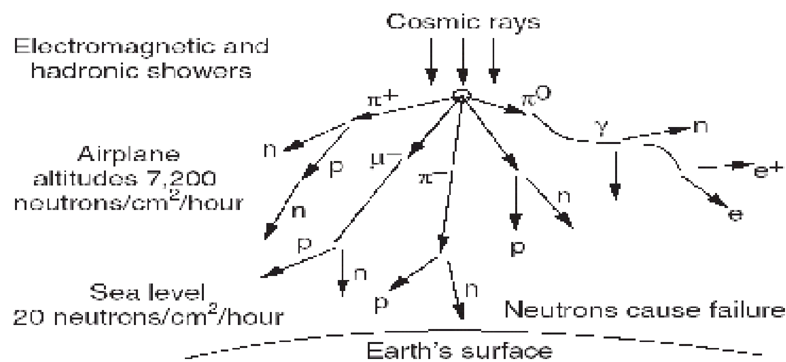


Figure 2.1: Cosmic shower through atmosphere.
[Adapted from [9]]

2.1 Particle Composition at Sea-level

The particles distribution at sea-level is dominated by neutrons, almost 90% [11]. Presence of pions, muons, and protons have been accounted, but are far less in comparison to neutrons. Pions and muons are involved in pion and muon captures respectively. Together they result in less than 100 FIT. More details on this can be found in [1]. Protons are positively charged particles and hence would readily recombine with an opposite charge. Although protons too have been reported to cause SEEs [19].

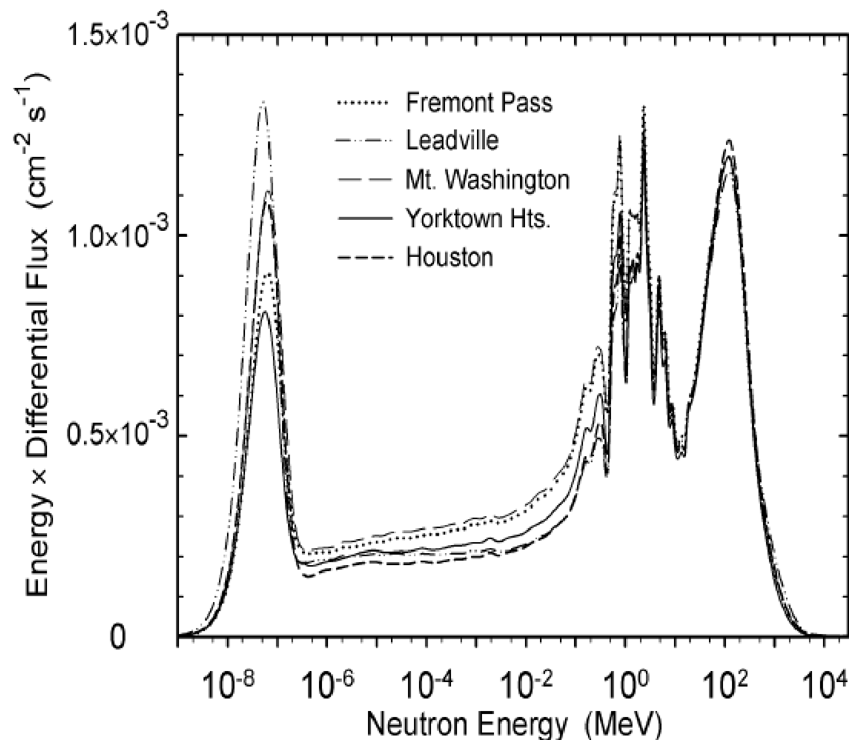


Figure 2.2: Terrestrial neutron flux at five different locations.
[Adapted from [1]]

Figure 2.2 is the neutron flux distribution across neutron energy. To illustrated the variation of neutron flux with altitude and latitude, the figure also compares the flux across five geographical locations. However, despite numerical variations, the pattern of distribution is fairly consistent. This pattern consists of three energy regions that dominate the plot. Neutrons at thermal energies (<1 MeV) are those which have lost all their energy and are under thermal equilibrium with other sea-level atoms [13]. At the other end of the spectrum are high-energy (>100 MeV) neutrons. These neutrons are the fraction of cosmic neutrons that have managed to travel through the atmosphere. The significant drop in their energy,

in comparison to the galactic neutrons, is because as they travel through the atmosphere, they are scattered by other atoms in the atmosphere. The scattering results in a loss of energy. At an energy level that is an order of magnitude lower than high-energy neutrons are spallation neutrons. Spallation is the process where neutrons are involved in a nuclear reaction with a target nucleus. The process of spallation may result in a neutron of much lower energy than the incident neutron. These low energy neutrons are typically of the order of 1-10 MeV. Also, The energy threshold on neutrons that can be absorbed is about 2-5 MeV. Hence neutrons that enter this region do not undergo any further reactions and are trapped in this energy band. This adds to the flux of neutrons in the spallation region.

2.2 Alpha Particles

Alpha particles present in the atmosphere lack the penetration power to upset the deeper layers of silicon. However, most circuits contain radioactive materials that emit alpha particles. These radioactive materials may be present in the packaging material, on-chip metals, or as impurities in the substrate. The starting energies of these alpha particles are about 5 MeV [10]. Based on the values from SRIM/TRIM [20] alpha particles travel a distance of a few micrometers in silicon. With respect to sub-micron feature sizes, this is adequate distance to reach the active region of the substrate.

Various sources have been identified as the source of on-chip alpha particles. Table 2.1 shows the contribution of some of the common on-chip sources of alpha particles.

Table 2.1: Common on-chip sources of alpha particles [1]

Source	Flux(α/cm^2-hr)
Processed Wafers	0.0009
Cu Metal (thick)	0.0019
Al Metal (thick)	0.0014
Mold Compound	0.024-<0.002
Underfill	0.02-0.0009
Pb-solders	7.2-<0.002
Ceramic package	0.0011

Chapter 3

Process of Error Manifestation

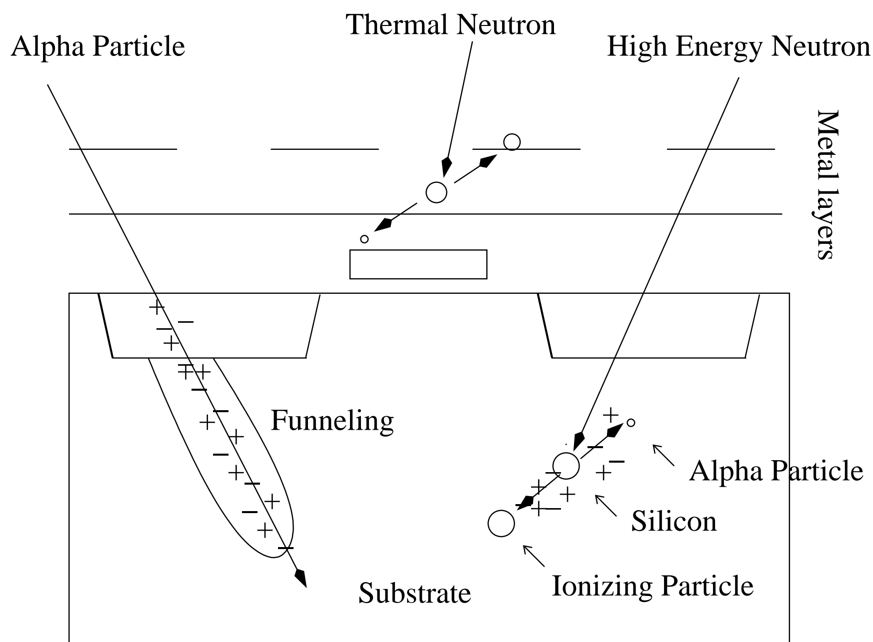


Figure 3.1: Particle induced error mechanisms.
(This has not been drawn to scale)

The interaction of external particles with a target material can be through (i) direct or (ii) indirect means, as seen in Figure 3.1. Direct interaction is by ionizing particles which have the capability to ionize a target atom as they pass through the material structure. Ionization is the ability of a projectile to eject electrons from target atoms by transferring energy. For example, at room temperature, silicon requires about 3.6 eV to be ionized. Neutrons, being electrically neutral, are incapable of directly ionization other particles.

However, their electrical neutrality allows them to move closer to the atomic nucleus. Hence, neutrons react by bombarding the target atom, resulting in nuclear fission. If the resultant products of the nuclear fission are ionizing particles, they are capable of generating an error through direct interaction.

3.1 Ion Induced Errors

The passage of ions through a material is described by linear energy transfer (LET). LET is an approximation of the energy transfered by an ionizing particle for every unit length it travels in a material. LET is a function of the initial energy of the projectile, and chemical properties of the ion and the target material. Also derived from LET is the stopping power of the projectile. A more detailed analysis on LET is available at [4, 6, 9]. Ziegler's SRIM/TRIM codes simulate LET for various particles and target materials [20].

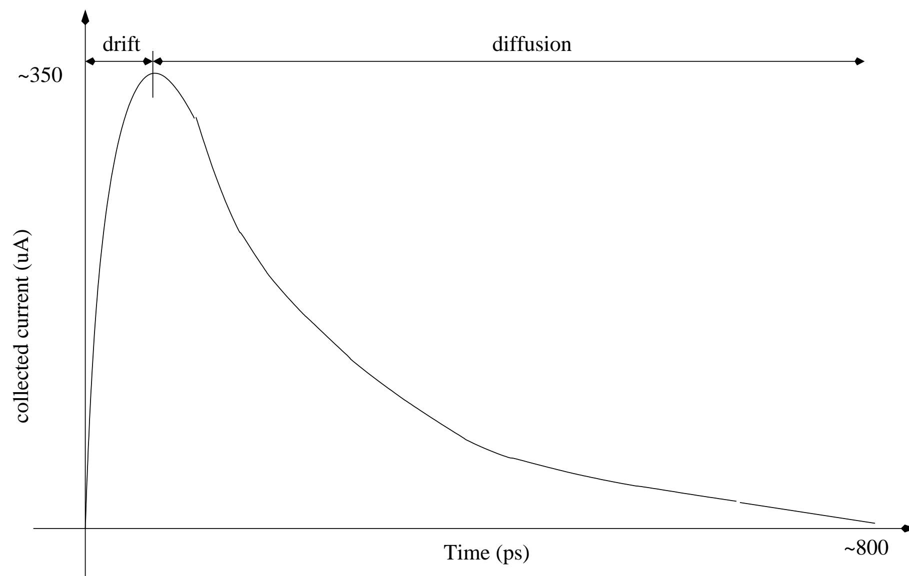


Figure 3.2: Collected current as a result of funneling.
(This has not been drawn to scale)

If a target atom's ionization energy is less than that obtained from the ionizing particle (characterized by the LET of the ionization particle), then the ionizing particle succeeds in ionizing the target atom. The process of ionization results in a sea of charge carriers. However, most of these charge carriers recombine due to Coulomb force. But, in the presence of an electrical field, some of these charge carriers are pulled away. The reverse biased junction of a transistor is most sensitive to a particle strike. At the instance of a parti-

cle strike, the electric field in the reverse biased junction collects these charge carriers by drift. Charges generated within the vicinity of the junction are collected through diffusion. Diffusion is much slower as compared to the drift mode of collection. As a particle strikes through a node, both drift and diffusion contribute to charge collection, resulting in a current pulse at that node. The entire mechanism is known as funneling [4]. Figure 3.2 is an approximation of the current pulse generated by funneling. The magnitude and duration of this pulse is dependent on the substrate doping. More information on funneling can be found at [4]

As a result of funneling a 1→0 transition can occur. Another mechanism, ALPEN, is capable of causing a 0→1 transition. ALPEN or alpha penetration is very similar to funneling. When a particle strikes through the channel of a transistor in cut-off, it can momentarily establish an electric field similar to the ON state of the transistor. The newly created conduction channel can produce a punch-through like current. ALPEN was first reported by Takeda et al. [17]

3.2 Neutrons in Silicon

Electrical neutrality ensures neutrons are not affected by the Coulomb forces that exist between charged particles. Neutrons interact with the nucleus in one of three ways, (i) elastic collision, (ii) absorption, and (iii) nuclear spallation [5]. The mode of reaction is dependent on the incident neutron energy and the microscopic cross-section of the atom. Also, in the context of SEE, only the first collision of a neutron needs to be considered because the mean free path of neutron in silicon is 2-10 cm [5]. Mean free path is the distance between two successive collisions of a neutron with different atoms.

Microscopic neutron cross-section is a quantity to represent the probability of a target atom to interact with a incoming neutron. It is measured in *barns*. 1 barn is equivalent to 10^{-24} cm^2. The product of the number of atoms in a unit area of a material and the microscopic cross-section (σ) is the macroscopic cross-section (Σ). Equation 3.1 describes the relationship between the two terms [5].

$$\Sigma = N\sigma \qquad (3.1)$$

where,

Σ = Macroscopic cross-section

σ = microscopic cross-section

N = Number of atoms

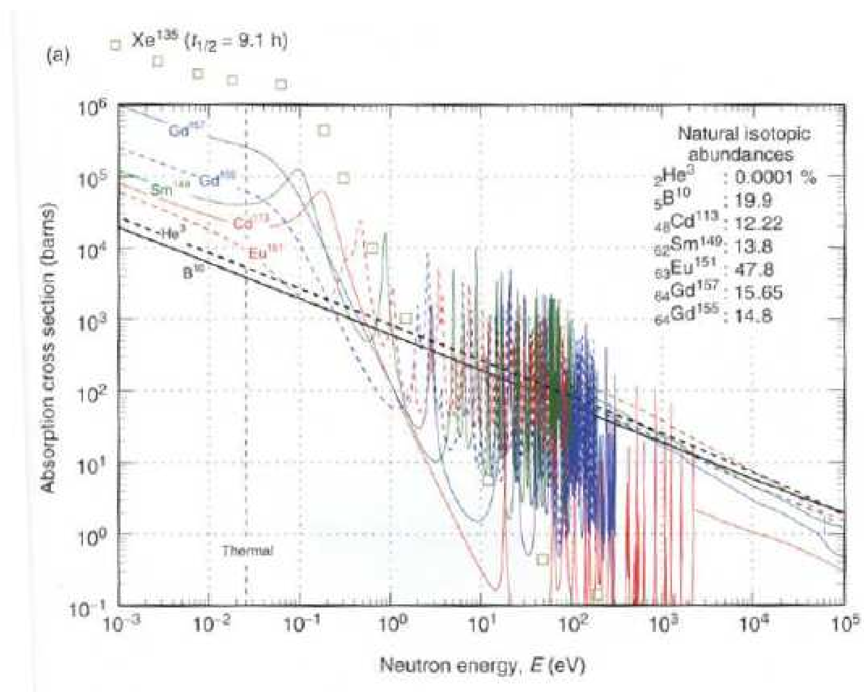


Figure 3.3: Neutron cross-section of selected material across neutron energy [Adapted from [5]]

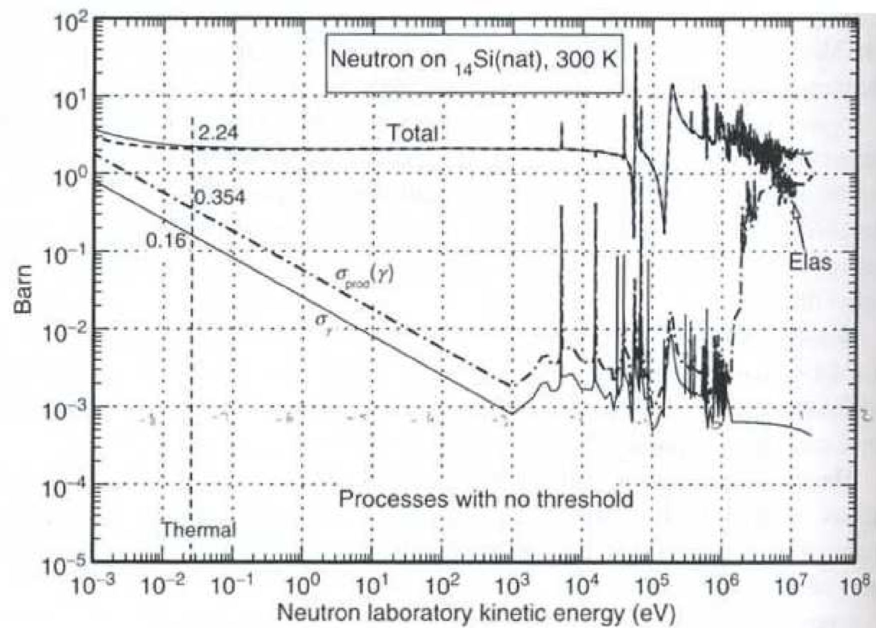


Figure 3.4: Neutron cross-section of silicon across neutron energy [Adapted from [5]]

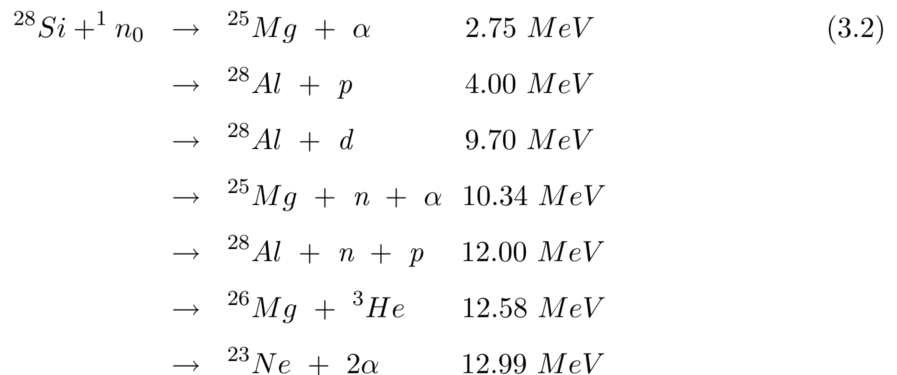
Figure 3.3 plots the microscopic cross-section across neutron energy for a few selected elements. A similar plot for silicon is as shown in Figure 3.4. Amongst the elements in Figure 3.3, boron-10 (^{10}B) is of significant interest. Boron is used as a dopant in integrated circuits. Compared to silicon, ^{10}B has a very high neutron cross-section at thermal energies. However, across the neutron energy spectrum, the neutron cross-section of ^{10}B drops significantly. In fact, at higher energies, silicon is far more likely to interact with neutrons.

BPSG, which contains boron, was an integral part of circuits until recently. Boron is an isotope that exits as 80% ^{11}B and 20% ^{10}B [7]. On absorbing thermal neutrons, ^{10}B produces an alpha particle and a heavy ion (^{7}Li) as reaction products. Both of the resultant particles are capable of inducing an upset. However, with the elimination of BPSG the error rate reduced significantly, as shown in Table 3.1.

Table 3.1: Contribution of BPSG to SRAM SER [8]

Contribution	0.25μm (with BPSG)	0.18μm (no BPSG)
Alpha Particles	4%	18%
High Energy Neutrons	15%	82%
^{10}B Fission	81%	0%
Total SER (A.U.)	7.5	1.0

At higher energies (> 1MeV) neutrons are not easily absorbed. They travel at higher speeds and impact the circuit by bombarding the nucleus. The possible reactions of neutrons with silicon atoms and their respective threshold energies are as shown in equation 3.2 [7].



$$\begin{aligned}
{}^{28}Si + {}^{1}n_0 &\rightarrow {}^{25}Mg + \alpha && 2.75\ MeV \\
&\rightarrow {}^{28}Al + p && 4.00\ MeV \\
&\rightarrow {}^{28}Al + d && 9.70\ MeV \\
&\rightarrow {}^{25}Mg + n + \alpha && 10.34\ MeV \\
&\rightarrow {}^{28}Al + n + p && 12.00\ MeV \\
&\rightarrow {}^{26}Mg + {}^{3}He && 12.58\ MeV \\
&\rightarrow {}^{23}Ne + 2\alpha && 12.99\ MeV
\end{aligned} \tag{3.2}$$

Every reaction produces one or more ionizing particles accompanied by other additional particles. Since the initial energy of these resultant particles are higher than the alpha

particles from on-chip radioactivity, the range of the neutron-induced ionizing particles are much larger. Furthermore, neutron interactions generate ionizing particles much closer to the active region. Thus, high-energy neutrons are a more effective error agent than on-chip alpha particles.

Chapter 4

Errors and Trends

The effect of scaling on soft error rate (SER) is challenging to analyze precisely. Reducing the operational voltage reduces the critical charge of a transistor, making it more susceptible to logical inversion through charge collection. However, shrinking feature size reduces the available active area. Further, the structure and functionality of a component can affect the SER, as shown in varying error trends in memory and logic.

4.1 Errors in Memory

Memory state in SRAM is maintained through a continuous regenerative feedback from cross-coupled inverters. Any glitch produced has to overcome the driving force of the complementary transistor. The refresh period of an SRAM cell is equivalent to the inverter's gate delay. SER in SRAM across technology generation is shown in Figure 4.1 [7]. The two show the error trends at the system level and at the bit level. System level SER is related to the integration density of SRAM. It accumulates the bit level SER over integration density. From a scaling perspective, bit level SER is more interesting. Also shown in the figure, in dotted lines, is the expected SER if the use of BPSG had been continued.

Early technology generations produced robust SRAMs. The reasons being high operational voltage and robustness through active feedback. However, voltage scaling results in an increase in SER. For example, in 90nm technology, an SRAM stores about 10 fc of charge, while the charge collected from an alpha particle is about 100 fc [11]. But a conscious attempt to reduce cell area has managed to contain the per-bit error rate in SRAM [7].

DRAM is amongst the most robust components. The data refresh rate in DRAM is much slower to provide the robustness than in SRAM. However, the use of three-dimensional capacitors has significantly increased critical charge and reduced collection efficiency. Further,

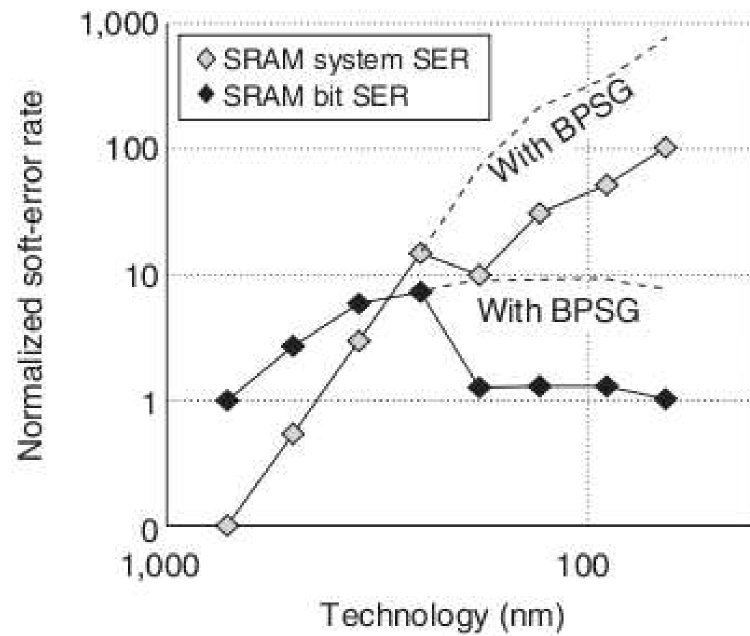


Figure 4.1: Error in SRAM with an without BPSG across technology generation [Adapted from [7]]

with scaling, the collection volume is reduced, thus resulting in a decrease in SER of DRAM. Figure 4.2 illustrates the SER trend in DRAM across technology [7].

4.2 Errors in Logic

Logic is a series of latches and combinational elements. For a fault in the combinational element to be latched, the faulty glitch has to first overcome the noise margin of the component. It must then have the logical path available to reach the latch. Subsequently, it must arrive in a manner that fits within the latching window. Even when the above conditions are satisfied, a glitch may still fail to propagate if the series of combinational elements degraded its signal strength. This effect is referred to as masking and is shown in Figure 4.3. Essentially thee kinds of masking are possible in logic [10],

- Electrical Masking - A transient glitch of a particle strike is attenuated by the subsequent gates in the logical path.
- Logical Masking - When a glitch is blocked from affecting the output because the output is determined by the other input signals.

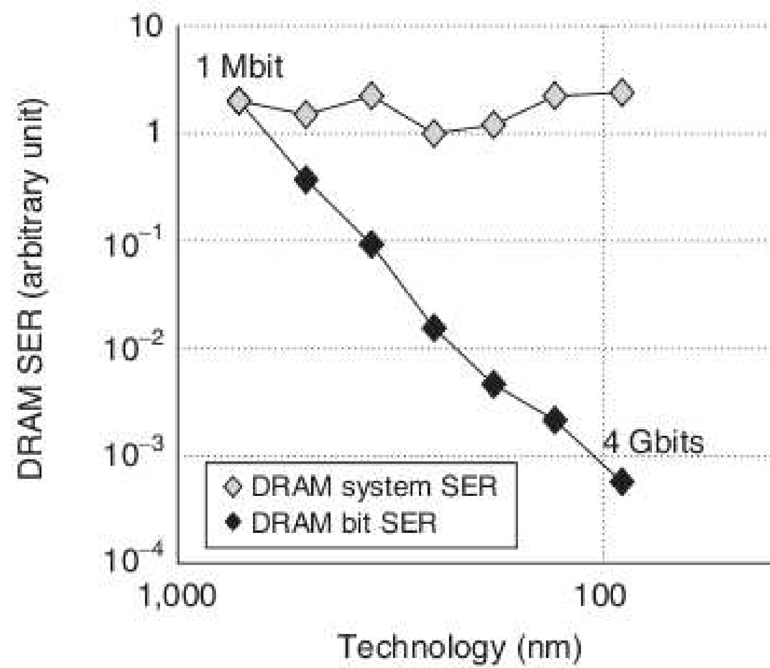


Figure 4.2: DRAM error trends as a function of technology generation
[Adapted from [7]]

- Latching Window Masking - The glitch fails to fall within the active region (temporal) of the latch.

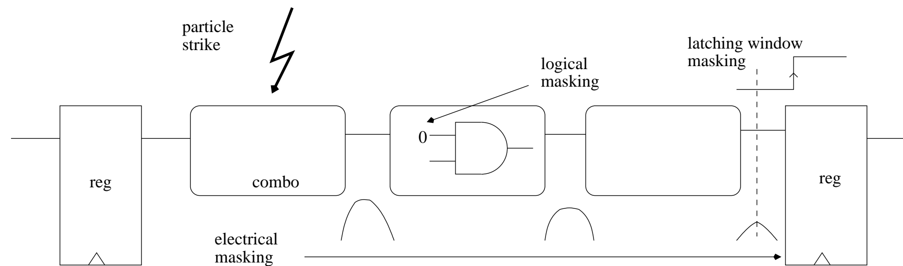


Figure 4.3: Three kinds of error masking in logic

Of course, with all these masking effects, a direct particle strike on the latch itself can result in an error. Between the latch and the logic, the error occurrence can be differentiated as synchronous and asynchronous. Synchronous errors are those occurring at the logic, since the error manifestation is dependent on clock. Latch errors are asynchronous since the error is from an asynchronous event, a particle strike.

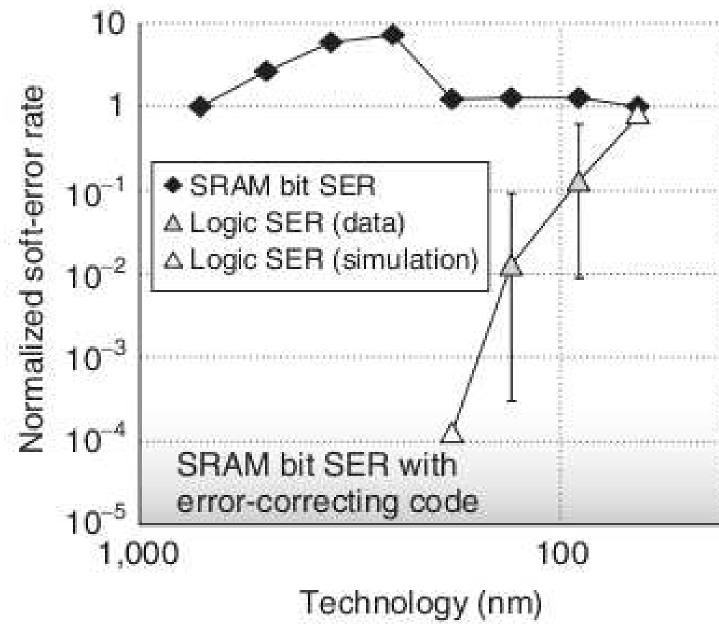


Figure 4.4: Comparing error rates in SRAM and logic components across technology [Adapted from [7]]

The scaling trends in logic are presented in Figure 4.4. Also included is the SER in memory for comparison. The steep increase in error rate of logic is attributed primarily to the increasing operational frequency and reduced propagation delay. Both of which present a higher probability for a glitch (introduced by a particle strike) to be latched. Baumann predicts that beyond 90nm, a larger fraction of the soft fails would be a result of latched transient events [7].

Chapter 5

Thin-film based Detection

From the discussion so far, high-energy neutrons continue to expose the vulnerability in CMOS circuits, a trend that increases significantly with each technology generation. Reducing errors rates can be achieved either by containing the error source, or by employing additional circuitry to provide redundancy or error correction. Shielding neutrons, as an on-chip solution is impractical [18]. The alternative is to contain the reaction mechanisms that lead a particle strike to cause an error. Most of these techniques are variations in substrate engineering. Silicon on insulator (SOI) shows promising trends in containing SER when compared to the bulk CMOS structure. SOI reduces the volume of substrate beneath the active region and hence inhibits charge collection [12]. Other techniques to reduce the charge collected include managing doping profiles and providing guard rings [7]. However, the enhancements achieved are poor in comparison to the additional cost and complexity [7].

The alternative to containing errors is error detection and redundant execution. Error correction circuitry can be added to provide additional information that can detect and reconstruct corrupted data. However, this technique may have limitations when extended to logic, as information in logic is less predictable when compared to memory. Redundant execution can reliably detect errors caused by particles. Unfortunately, they are more expensive in area and power.

From Figure 3.3 and Table 2.1, the number of particles capable of producing errors are low when compared to on-chip propagation speeds. In fact as an approximation, the mean particle flux seen by a die of area 150 mm^2 can be calculated as 1/6000 seconds, or roughly one every trillions of cycles. Hence, if a capability to detect the passage of neutrons exists then, a feedback about the particle strike can allow the system to roll back to a previously saved stable configuration. Figure 5.1 details this idea. Although a roll back will occur even if the detected particle fails to cause an error, given that a particle strike is an exceedingly

rare event in comparison to the on-chip activities, the performance degradation from a roll back would be insignificant - provided the detection latency is reasonably short. However the system would have to maintain a fall back state and have a continuously operating detector. The rest of this chapter studies the feasibility of the detection layer.

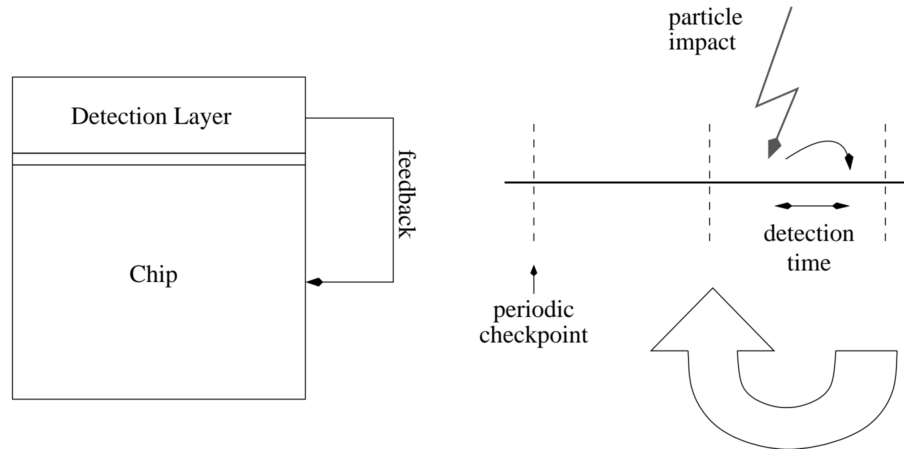


Figure 5.1: Detection based error protection

5.1 Exploring Detection Mechanism

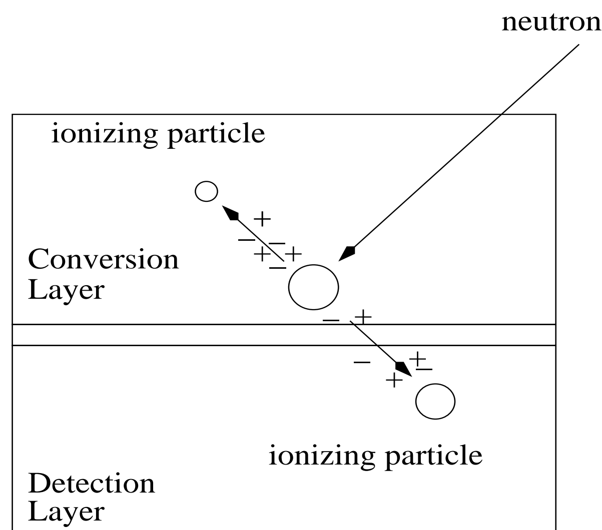


Figure 5.2: Visualization of the detection scheme

The detection scheme shown in Figure 5.1 is detailed in Figure 5.2. The detector consists of a conversion layer over a detection layer. The conversion layer interacts with an incoming

neutron to produce a reaction that can easily be tracked or monitored by a detection layer. The key is to build a conversion layer that has a high probability of interacting with neutrons. For instance, to increase the mean time to failure (MTTF) by an order of magnitude, we need to detect more than 90% of the incoming particles. Since the probability of a neutron interacting with a material is high if the neutron cross-section of the material, for a given incident energy, is high, the conversion layer must have a high neutron cross-section at higher energies (1 MeV) of neutrons. The detecting layer is a material that suitably reacts with one or more of the reaction products in a manner which can be monitored.

Detection, however, can be relatively easily achieved, especially if the resultant particles are ionizing particles. Weakly driven reverse biased junctions are vulnerable to charge collection from the passage of an ionizing particles. Hence, unprotected memory or even a reverse-biased pn junction would qualify as a detection layer. Forward biased junctions maintain much higher voltages as compared to the voltage generated by the error. Hence the occurrence of an error may go undetected.

In general, if F neutrons pass through the thin film, X neutrons may react with the conversion layer. This number is proportional to the neutron cross-section of the conversion layer. Assuming X relevant resultant products are realized from these X reactions. Of these if Y particles get absorbed in the conversion layer, X-Y particles will reach the detection region. Of the X-Y particles reaching the detector, Z particles may go unnoticed by the detection mechanism. Hence of all the X particles that react with the conversion layer, X-Y-Z particles are available for detection. Also possible is the fact that a fraction of the F-X neutrons reacts with the detection layer. Overall the efficiency of detection can be stated as,

$$\text{efficiency} = \frac{((X-Y-Z)+a(F-X))}{F}$$

Assuming all neutrons interact with either the conversion or detection layer, a fraction of these ionizing particles may go undetected by the detector. Hence, the process of detection can introduce new errors. The number of undetected errors will be,

$$\text{Thin-film introduced errors} \approx \text{bZ}$$

where,

$$
\begin{aligned}
\text{F} &= \text{Incident neutron flux}\\
\text{X} &= f(\Sigma_{ConversionLayer})\\
\text{a} &= f(\Sigma_{DetectionLayer})\\
\text{Y} &= f(LET_{ConversionLayer}, \text{d})\\
\text{Z} &= f(LET_{DetectionLayer}, \text{fidelity of the detector})\\
\text{b} &= f(LET_{Silicon})\\
\Sigma &= \text{Macroscopic cross-section}\\
\text{d} &= \text{depth of particle strike in the conversion layer}
\end{aligned}
$$

In the above analysis, reducing the newly introduced errors is possible only by reducing Z, since b is almost fixed for silicon. Reducing Z can be achieved by either improving the detector efficiency or increasing Y. Y is the fraction of the ionizing particles which get do not reach the detection layer. Increasing Y can be achieved by increasing the thickness of the conversion layer. This would also increase the volume of conversion layer available for interacting with neutrons. However, neutrons exhibit a mean free path between successive collisions. For example, in silicon this value is about 2-10 centimeters [5]. Hence, careful design is required to ensure that the thickness of the conversion layer is not comparable to the mean free path of neutron in the conversion layer.

For a given range of values an incident neutron can take, the neutron cross-section and LET of the incident particle, in the conversion layer, are properties of the chemical composition of the conversion layer. Of course, the thickness of the conversion layer can be optimized too, but variations in thickness are constrained by on-chip feasibility. Hence, the key to designing thin-film based detection is Σ, or the material composition of the conversion layer.

5.2 Analysis of Practicality

The key challenge is to reduce the number of neutrons not converted by the conversion layer F-X. Given a conversion layer of thickness x, we can compute the flux absorbed by the layer using Equation 5.1 [14, 15].

$$
\begin{aligned}
Flux(x) = F - X &= F - Fe^{-\Sigma x}\\
&= F(1 - e^{-N\sigma x})
\end{aligned}
\tag{5.1}
$$

where,

F	=	Initial Flux
Σ	=	Macroscopic cross-section
N	=	Number of atoms per unit area
σ	=	Microscopic cross-section

In the equation above, three parameters control the variation of the neutron flux with depth: depth of the conversion layer, neutron cross-section of the material, and number of atoms per unit area of the material.

Revisiting a previous graph, Figure 3.3, which compares the neutron cross-section of a few selected materials, most elements or their isotopes tend to show high neutron cross-section at thermal energies but drastically lose the ability to interact with neutrons as the neutrons reach the higher end of the energy spectrum. In fact, from the spallation region onward, the neutron cross-section exhibited by silicon is far higher than that of boron-10. The neutron cross-section for silicon across neutron energy is shown in Figure 3.4.

As an example, consider a silicon based conversion layer. Silicon has a microscopic cross-section of, approximately, 10 barns. Its crystal is a diamond-like structure and the number of atoms in a unit centimeter-square can be assumed as 10^{15} atoms/cm^2 [16]. Using Equation 5.1, Table 5.1 calculates the neutron flux across the thickness of silicon.

Table 5.1: Flux at various depths of silicon

thickness x	Flux(x) (% of F)
1 μm	99.9999999999
1 mm	99.9999999
1 cm	99.999999
10 cm	99.99999

From the results in Table 5.1, it is impossible to achieve any detection by growing silicon on-chip as a conversion layer. Viewed from a different angle, to select a material and build a conversion layer of 1 cm thick that converts 90% of incoming neutrons (F-X = 10% F), the required σ is almost 10^9 barns. Therefore, it is unlikely such a conversion layer can be built from known materials.

Chapter 6

Conclusion

Protection against SEE is a critical design decision. Technology scaling and increasing integration densities have been constantly pushing the limits on reliability. This thesis presented a brief overview of some of the key aspects in this field.

Particle flux at the sea-level was analyzed. High-energy neutrons and alpha particles contribute to most particle-induced errors. Alpha particles from on-chip components continue to pose a design challenge. However, low alpha materials are available to minimize the alpha particle flux. Further, since alpha particles can be shielded easily, error reduction can be achieved by careful design techniques, such as, keeping the active region away from alpha particle sources.

Most error-inducing neutrons fall into three distinct regions; thermal, spallation, and high-energy neutrons. Since the removal of on-chip boron-10, thermal neutrons have been concluded as ineffective in causing an upset. However, high-energy neutrons continue to make CMOS transistors more vulnerable.

This thesis proposed the thin-film based detection as a cheaper alternative to redundant execution and radiation hardening. The goal was to analyze the feasibility of providing a significant error reduction at a much cheaper price. Projectile neutrons are to hard shield. Hence an attempt to monitor the passage of neutrons was studied. However, the given knowledge of available materials restrict the viability of this option.

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