Decoupling Capacitance

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Abstract—**Decoupling capacitors (decap) are often used to filter out noise in the power distribution system (PDS). Decaps acts as a local source of energy for a short period. With the scaling of CMOS technologies the power supply voltage is lowered, clock frequency has gone up, and more functionality is integrated on-chip resulting in higher simultaneous switching noise (SSN). As a result signal integrity of on-chip power supply has become a major concern. Placement and sizing of decaps, effective utilization of on-chip whitespace, resonant free voltage responses for a wide range of frequencies are some of the key challenges faced with the shift towards deep submicron regime.**

I. INTRODUCTION

Decoupling capacitors known as "charge reservoirs" are placed between power and ground lines to maintain low target impedance and to reduce the noise in power distribution network. Low impedance and resonant free response are two requirements for maintaining power and signal integrity of the PDS. Power distribution system (PDS) spans different levels of hierarchy consisting of voltage regulator module, power distribution network on board, on package and on-chip. Hierarchical placement of decaps is generally used to confine the output impedance by terminating the power current loop closer to the load as frequency increases. With technology scaling as devices are of smaller feature size, have faster switching speed, and higher integration density, signal integrity and noise in the power distribution system have become a major concern [1]. Several techniques comprising of topology optimization, wire sizing, on-chip voltage regulation and deployment of decoupling capacitors are considered for relieving power supply noise. To ensure minimum power supply noise, PDS should exhibit small output impedance at the load or current sink. Lowering the impedance helps in reducing the IR and L*di/dt* noise over the power supply network. Hierarchically placed decaps needs to be sized progressively to avoid unwanted antiresonance to occur within the specified frequency range. The impedance at the antiresonant frequency is increased by quality factor of the LC tank circuit formed by parallel capacitors. The most effective way to reduce the peak of antiresonance is to minimize inductance by placing low effective series resistance (ESR) capacitor on low inductive pads or place multiple decaps with progressively decreasing value. The problem of noise integrity has become more complicated with multiple power supply voltages. Noise coupling or interaction between the two PDS becomes important parameter for designing decaps. Technology scaling has enabled on-chip integration of capacitors with varied oxide thickness. Thinner capacitors have low capacitance per unit area of decap, but can significantly increase the leakage current of decap. With several design objectives at hand, proposals to efficiently design, plan, size, and deploy decaps to meet target impedance and noise constraints.

The rest of the paper is organized as follows. Decap planning, sizing and allocation algorithms for power supply noise suppression are presented in Section II. Methodology for designing decap in multi-voltage power distribution system is presented in Section III. On-chip High-K MIM decap and socket level decap platform for power integrity is presented in Section IV. Some specific conclusions and future work are summarized in Section V.

II. ON-CHIP DECOUPLING CAPACITANCE BUDGET

On-chip power supply network can be modeled in several structural types e.g. routed network, mesh, grid, cascaded power and ground rings. Power supply network chosen for noise estimation is shown in Figure 1, where each segment is modeled as a lumped RLC element, and the complete mesh is modeled as a pseudo-distributed RLC network. The circuit blocks are modeled as time-varying current sinks that draw current from the VDD sources. Allocation of decap to each module is based on power supply noise it experiences [1]. To estimate the noise, the voltage difference between connection point and its neighboring supply pin is calculated using (1):

$$V_{noise}^{(k)} = \sum_{P_j \in T^{(k)}} (ij * RP_{jk} + LP_{jk} * di_j / dt), \qquad (1)$$

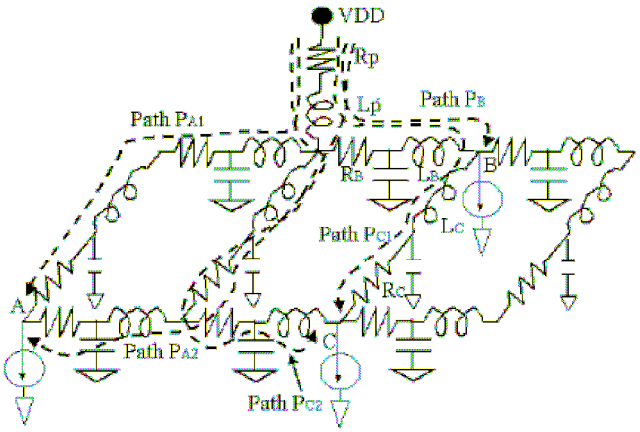

Figure 1: Model of power supply mesh network

where i_j is the current flowing along the path P_j. R_{Pjk}, L_{Pjk} denote the resistance and inductance of P_{jk}. To calculate the size of decap the estimated power supply noise of module k is scaled by ϕ times the tolerable noise limit $V_{noise}^{(limit)}$ by reducing the current flow through the network by $1/\phi$. The decap required for each circuit module can be estimated as:

$$\phi = \max(1, V_{noise}^{(k)} / V_{noise}^{(\lim)}), \qquad (2)$$

$$C(k) = (1 - 1/\phi) * Q^{(k)} / V_{noise}^{(k)}, k = 1,2,...,M, \qquad (3)$$

The problem of white space allocation is solved using linear programming technique subject to linear inequality constraints by converting the decap budget for each circuit module to the equivalent area of silicon required to fabricate the decap using $S^{(k)} = C^{(k)} / C_{ox}, k = 1,2,....,M$, where, C_{ox} represents the unit area of MOS capacitor. Extending to decap sizing algorithm proposed in [1], the authors of [2] proposed an algorithm to measure effective decap distance for noise and leakage reduction. The power supply network considered for noise estimation is resistive mesh, and the size of unit decap is calculated using greedy approach, assuming block would draw all of its switching current from its decap. As the blocks can potentially draw current from all nearby decaps, this approach made use of non-adjacent whitespace for decap allocation. Decap is sized based on resistance between decap and non-adjacent current module. Voltage supplied to the block during switching is: $V(t) = V_{dd} - V_{noise} + V_{noise} (R_d/R_c + R_d) * e^{-t/(Rc+Rd) C}$, where $V_{noise} = R_d * I_h$, I_h is the current drawn during switching interval of time (t_s). Decap requirements of a particular block can be calculated using the above expression. For finding the actual decap for a block the base decap calculated using greedy approach is multiplied by effective distance $\gamma_{eff} = C(Rc)/C(0)$. For detection of whitespace in a floorplan longest path tree calculation based on vertical constraint graph is computed. If the boundaries of blocks at different levels are not incident on each other, then there is a whitespace. For decap allocation and sizing problem generalized min-cost network flow is modeled with dual oxide thickness capacitors. Thin oxide decap are placed in extremely noisy spots and thick oxide decaps are placed at the areas with less noise so as to minimize the gate leakage current [10]. Table 1 illustrates that configuration F is the best optimal configuration meeting the worst-case noise constraint of 200 mV and reducing the gate leakage power by 61 per cent.

The most comprehensive work on decap sizing and placement is [3]. Effective radii of an on-chip decap is calculated using two design parameters, target impedance (during discharge) and charge time before the next switching event as shown in Figure 2. Decap must be placed such that both effective radii criteria are met otherwise the current load should be partitioned. The maximum effective radius $d_z^{\max}$ determined by target impedance constraint is inversely proportional to the current load requirements and to the impedance of a unit length line $\sqrt{r^2 + \omega^2 l^2}$ where r, l is the resistance and inductance per length, and ω is an equivalent frequency. After the discharging of decap, decap must be charged again to meet the current requirements during next switching event otherwise decap will gradually deplete with time. Closed loop RLC circuit is used to determine the current flow through a decap during charging phase. The KVL expression for the circuit current is given by $L\frac{di_{ch}}{dt} + Ri_{ch} + \frac{1}{C_{dec}}\int i_{ch} dt = V_{dd}$. The effective distance based on the charge time is determined by differentiating the above expression and calculating for voltage at decap during the charging phase by integrating the charge flow through the decap from zero to charge time t_{ch}.

Decoupling Capacitors	Thin-oxide Area (mm^2)	Transient Noise (mV)	Leakage Power (W)
A	17.8	191	26
B	16.7	191	25
C	13.3	193	20
D	12.2	193	18
E	8.1	197	12
F	6.7	198	10
G	0.0	232	0

Table 1: Power supply noise comparison

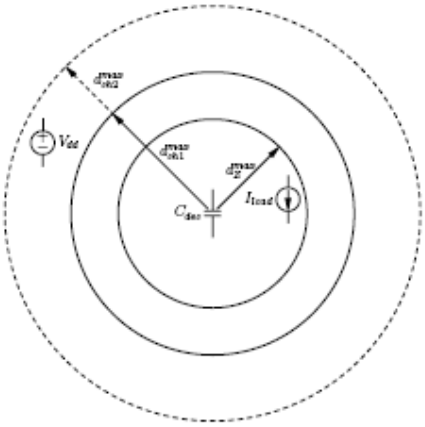

Figure 2: Effective Radii for an on-chip decap

The effective distance determined by the charge time is inversely proportional to C_{dec}^2. Finally, the on-chip decap should be distributed across the circuit to provide the required charge for each functional unit.

III. Decaps for Multiple Power Supply Voltages

Multiple power supply voltages are often used for decreasing power consumption in high performance systems, without affecting the circuit speed. In such systems the parasitic capacitance or decoupling capacitance between the two power supplies couples the system, causing power and signal integrity issues. Schematic representation of PDS with multiple power supplies is shown in Figure 3. The location of antiresonant spike depends on the ratio of Effective Series Inductance (ESL) [4]. To shift unwanted antiresonance spike to a high frequency either C_2 should be decreased or the overall inductance ESL should be decreased illustrated in Figure 4.

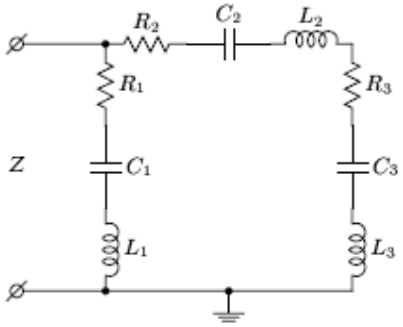

Figure 3: PDS with two supply voltages and decap

As shown in Figure 3, multiple power supplies are generally coupled so the decap placed between the two power supplies (C_2) must be designed to satisfy voltage transfer function constraint (4) to produce over-shoot free response.

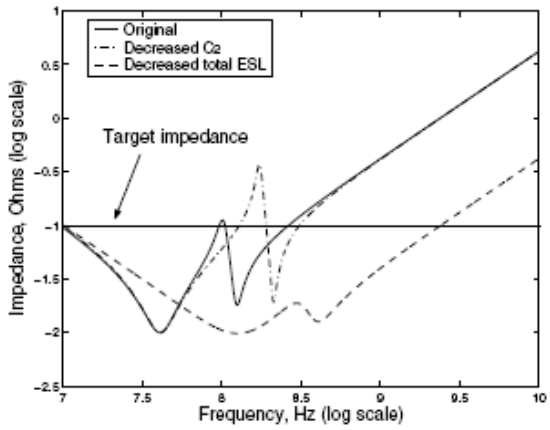

Figure 4: Impedance of a PDS with dual power supply

$$|Kv| \le \frac{r * V_{dd1}}{V_{dd2}}, \qquad (4)$$

where V_{dd1} is a lower voltage power supply, r is the allowed ripple voltage and V_{dd2} is a higher voltage power supply. $|Kv|$ is chosen to be less than or equal to effectively decouple a noisy power supply. For frequencies smaller the break frequency, the magnitude of the voltage transfer function is appr. C2/C3 decreases with decreasing ESL and decap is shown in Figure 5. For frequencies greater than the break frequency the magnitude of the voltage transfer function is appr. L3/L2 reduces with increasing ESL and decap [5].

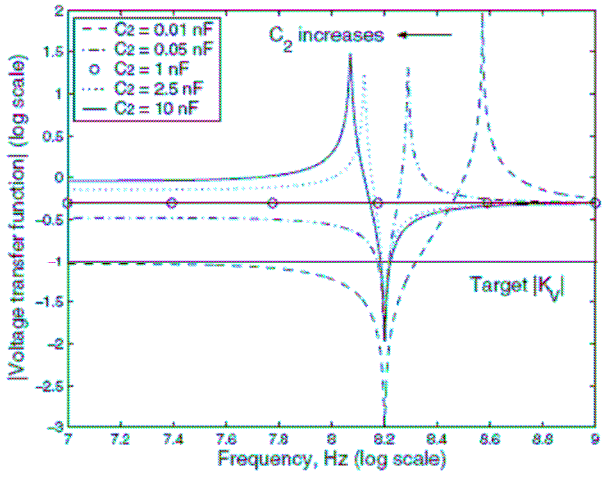

Figure 5: To maintain voltage transfer function below .1 for frequencies smaller than the break frequency. R_2=R_3= 10m Ω , C_3= 1nF and L_2=L_3=1nH.

IV. On-Package Decoupling Capacitor

The signal integrity issues at package level are mainly due to SSN of several IO drivers, high IO power distribution network inductance, mismatched traces and voltage fluctuations in power and ground terminals due to SSN. As seen above, effectiveness of decap is limited by the associated parasitic effective series resistance and effective series inductance. On-die High-K MIM decap [9] and CapCore [7] have emerged as an alternative to the existing package and board level capacitors. High-K MIM capacitors have high dielectric leakage due to thin gate oxide, but are more effective compared to the traditional thick gate-oxide capacitance in providing resonant free low impedance over a wide range of frequency. MIM decap are physically located below the thick metal layer which is mainly used for power routing, clock distribution and IO signals. The authors of [9] have shown significant improvements in noise, speed and power by using high capacitive density on-die High-K MIM decaps as compared to gate oxide decaps.

To meet similar design requirements of increasing the effectiveness of on-package decaps CapCore model is proposed. In this new configuration, decap is placed within the substrate and interposer effectively reducing high inductive loop by bringing decap closer to the die as shown in Figure 6. With this scheme the decap requirements of two pads, two vias, plane connections, some traces and PCB area can be liberated. This newly liberated space reduces congestion, simplifies routing, lowers crosstalk, and reduces discontinuities.

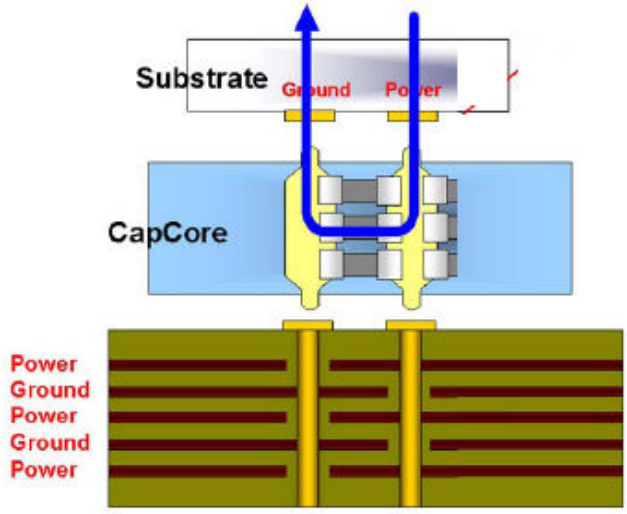

Figure 6: Decoupling Loop with CapCore interposer

V. Conclusions and Future Work

At high frequency on-chip decap are used to reduce switching noise introduced due to internal circuit switching during a given cycle time. On-package and on-board decaps are more efficient in controlling noise in multiple cycles at medium and low frequencies. Power supply noise estimation model, which models noise in distributed RLC power plane is introduced. Different algorithms for placement of on-chip decaps either adjacent to the "hot-spot" or distributed based on the effective radii determined by target impedance and charge time are discussed. Decap designing strategy for optimally damped circuit with over-shoot free voltage response is presented. The prospective research area for the near future could be placement and sizing of decap in 3D integrated chips, tools for modeling noise and impedance characteristics in power mesh for 3D integrated chips with multiple power domains. In the future scaling of CMOS technology will enable several package level design options for designing decaps similar to the present High-K MIM decap with thinner oxide.

VI. References

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