The Rochester Cube and Other 3-D Circuits for Clock and Power Delivery

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November 22, 2009

3-D Architectures for Semiconductor Integration and Packaging
An Increasing Interest in 3-D ICs

![Graph showing increasing number of publications from 2001 to 2008]

- Source: IEEEExplore

Applications of 3-D Integrated Systems

- Lab on a chip
- Real-time image processing systems
- Multi-core 3-D architectures

Presentation Outline

• Three-dimensional (3-D) integration
• Physical design issues in 3-D integration
• The Rochester cube
• 3-D power delivery
• 3-D logic on memory
• 3-D optical interconnect
• Conclusions
Primary Advantages of 3-D Integration

- Integration of disparate technologies
  - No yield compromise
  - Greater functionality
- Number and length of global interconnects are reduced
  - Reduction in interconnect power
- Innovative architectures
  - Dedicated NoC plane for IP block level communication


Break Through the Interconnect Wall

- Exploit improvements from device scaling
- Greater speed, lower power dissipation, lower noise levels
- A novel solution is required
- High functional capacity
- Offer inherent heterogeneity
Spectrum of Challenges in 3-D ICs

Manufacturing
- Plane alignment and bonding
- Through silicon vias

Testing
- Pre-bond testing
- Post-bond testing

Design
- Interconnect design techniques
- Thermal management techniques
- Physical design techniques

Objectives for 3-D CAD Tools

“New design tools will be required to optimize interlayer connections for maximized circuit performance…”

TSVs
- Density / consume silicon area
- Impedance characteristics

Heterogeneity
- Interdie process variations
- Disparate technologies

Interconnect length
- Longest nets in a 3-D system

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Interconnect Design Issues in 3-D ICs

• Global signaling
  – Clock and power distribution
• Noise aware design methodologies are needed
  – Due to the adjacency of the physical planes

Effective signal, clock, and power delivery is essential
3-D Floorplanning and Placement

- Third dimension greatly increases the solution space
- Adopt a two-step solution

1st step

2nd step

Through Silicon Via (TSV) Placement

- Treat TSVs as circuit cells
  - Use weighted average distance to determine final via location
- Place the cells of each plane separately
  - Including vias
Delay Dependence on TSV Location

- Determine the via location that minimizes Elmore delay
  - Closed-form solution

Interconnect parameters
- \( r_1 = 76 \, \Omega/mm \)
- \( r_2 = 53 \, \Omega/mm \)
- \( c_2 = 223 \, \text{fF/mm} \)
- \( c_3 = 279 \, \text{fF/mm} \)
- \( c_{13} = 1.674 \)
- \( I_v = 20 \, \mu m \)
- \( n = 2 \)
- \( R_s = 410 \, \Omega \)
- \( C_s = 180 \, \text{fF} \)

Minimum

TSV Characterization / Design

- Impedance characterization of TSV
- Physical models of TSVs
  - Distributed vs. lumped models
  - Closed-form expressions
- Circuit design techniques
  - Repeater insertion before and after via
  - Return path requirements to minimize loop inductance
- Inductive and capacitive coupling noise between TSVs
  - TSV-to-TSV shielding methodologies

• Equations model TSV electrical characteristics
  – TSV diameter $D$ and length $L$
    • $0.5 < \text{Aspect ratio} < 9$
  – Distance of TSV from ground plane $S_{gnd}$
  – Spacing $S$ to neighboring TSVs
    • Capacitive coupling
    • Loop inductance

TSV Impedance Models

• DC Resistance: < 2%
• 1 GHz Resistance: < 4.5%
• 2 GHz Resistance: < 5.5%

• Self Inductance $L_{11}: = 8\%$
• Mutual Inductance $L_{21}: = 8\%*$

• Capacitance to ground: = 8%
• Coupling Capacitance: = 15%*

* Error in mutual inductance and coupling capacitance ratios and distant vias as both conditions prod
Complex design issues
- Limited metalization layers for critical IC components
- Clock network design constrained by skew and jitter
- Power delivery under noise constraints for target impedance

Complex design issues have become even more complex
- Vertical dimension adds to design complexity
- Clock network design constrained by intra-plane and inter-plane skew and global clock jitter
- Power delivery to multiple planes with potentially different voltage requirements
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3-D Clock Distribution and Power Delivery

Clock Network  Power Delivery
Clock Distribution Networks

- Clock signal is the “heart” of a synchronous circuit
- Deeply scaled technologies
  - Increasing frequencies
  - Greater process variations
  - Clock skew, jitter need to be carefully managed
- Hierarchical clock distribution networks
  - Global networks
    - H-tree, X-tree
  - Local networks
    - Meshes

Clock Signal Distribution for 3-D ICs

- Multiplane system
  - Process variations
- Different forms of 3-D integration
  - System-in-Package (SiP)
  - 3-D ICs (high density vias)
- Clock signal distribution under pronounced thermal effects
3-D Clock Distribution Network Test Chip

- Clock network on the 2nd plane is rotated by 90° to eliminate inductive coupling

Block Diagram of the 3-D Test Circuit

- Each block includes
  - Identical logic
  - Different clock distribution network
- Objectives
  - Evaluate clock skew
  - Measure power consumption
- Area - 3 mm × 3 mm
Logic Circuitry

- Current loads mimic various switching patterns
- Control logic periodically changes the connectivity among the input and output ports

MIT Lincoln Laboratories 3-D IC Fabrication Process

- FDSOI 180 nm CMOS process
  - Three plane process
  - Three metal layers for each plane
  - Back side metal layer for planes 2 and 3
  - One polysilicon layer
- 1.75 µm × 1.75 µm cross section of TSVs
  - For the 2nd 3-D multiproject

*Massachusetts Institute of Technology Lincoln Laboratory, FDSOI Design Guide*
Two Digital & One RF 180-nm 1.5V FDSOI CMOS Tiers

3DM2 Process Highlights
- 11 metal interconnect levels
- 1.75-µm 3D via tier interconnect
- Stacked 3D vias allowed
- Tier-2 back-metal/back-via process
- 2-µm-thick RF back metal
- Tier-3 W gate shunt
- Tier-3 silicide block

Cross-Section of 3-D Interconnect

• Plane 3
• Plane 2
• Plane 1
• Interplane via
Second 3D IC Multiproject Run (3DM2)
(Three Tiers of 180-nm 1.5-volt FDSOI CMOS)

- 3DM2 run announced (March 2006)
- 3D design kits released (April 2006)
  - Mentor Graphics (MIT-LL)
  - Cadence (NCSU)
  - Tanner Tools

3DM2 Submissions (October 2006)

### 3D Circuits
- FPGA, stacked memory (SRAM & CAM),
- asynchronous microprocessor, FFT with on-chip memory, multi-processor chip with high-speed RF interconnect, ASIC with DC-DC converter, reconfigurable AE modulator, decoder with 3-cube torus network, self-powered and mixed-signal RF chips

### 3D Imaging Applications
- ILC pixel readout, high-speed imaging FPA, 3D adaptive image processor, artificial bio-optical sensor array, 3D retina, 3D-integrated MEMS biosensor, sensor lock-in-amplifier

### 3D Technology Characterization
- 3D signal distribution, 3D interconnect methods, parasitic RF & 3D radiation test structures

3DM2 Participants (Industry, Universities, Laboratories)

| Cornell | Minnesota | SUNY |
| Fermi Lab | NCSU | Tanner |
| Idaho | NRL | Tennessee |
| Intel | Pittsburgh | UCLA |
| Johns Hopkins | RPI | Washington |
| Lincoln Lab | Rochester | Yale |
| Maryland | Sandia |

MIT Lincoln Laboratory
Second 3D IC Multiproject Run (3DM2)
(Three Tiers of 180-nm 1.5-volt FDSOI CMOS)

Fabricated 3-D Test Circuit

- Full custom design
- ~120K transistors
Clock Signal Path in the Investigated Blocks

- Output from C
- Output from B

Clock and Data Waveforms

- Output bit at 1 MHz
- Clock output at 1.4 GHz from the 3rd plane

Clock Skew and Power Measurements

Maximum clock skew [ps]
- 130.6 ps
- 260.5 mW
- 8.5 mW
- 168.3 mW

Power consumption @ 1 GHz [mW]

Topography

- Lowest power
- Moderate skew

Dr. Vasilis Pavlidis


“15 Minutes of Fame”

Science News

3-D Computer Processor: 'Rochester Cube' Points Way To More Powerful Chip Designs

ScienceDaily (Sep. 17, 2008) — The next major advance in computer processors will likely be the...

First 3D processor runs at 1.4 Ghz

Researchers create first true 3D processor, turns chips into cubes

Dr. Vasilis Pavlidis

US university claims creation of first, true chip

Scientists at the University of Rochester have created what they claim to be the first three-dimensional computer processor, which could be a key component in future computers.

Rochester cube processor

The University of Rochester is in the final stages of making the three-dimensional computer processor.
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3-D Clock Distribution and Power Delivery
Effective Power Delivery Will be Essential

• All but one of the planes are located next to the P/G pads
  – TSVs convey current to other planes
• Decoupling capacitance can be placed within or on a nearby plane
• Multiple, distributed power supplies will be necessary
  – Due to thermal issues
  – Heterogeneous technologies
  – Lower power consumption

Power Delivery Test Chip
Design Objectives

• Blocks P1 - P3
  – Three different power distribution networks
  – Investigate noise within each power network
• Block DR
  – Distributed rectifier for on-chip DC-to-DC buck converter
Power Distribution Network Topologies for 3-D ICs

P1: interdigitated
- 3-D vias on periphery

P2: interdigitated
- 3-D vias on periphery and through middle

P3: gnd planes on plane 2, interdigitated on planes 1 and 3

Noise Detection Circuitry

- Voltage sense amps used to detect and measure noise on each plane for each power distribution topology
  - Noise analyzed on both $V_{DD}$ and ground lines

CM = current-mirrors, RO = ring oscillator, RNG = random number generator, VSA = voltage sense amp
Standard Buck Converter

- Generates an output supply voltage
  - Smaller than the input supply
- Power MOSFETs produce an AC signal at node A
- AC signal is filtered by rectifier
  - Second order low pass band LC filter
- Filter passes the DC component of the signal and a residue
  - Composed of high frequency harmonics
- Buck converter produces an output DC voltage at node B
  - Equal to product $D V_{SAT}$

Distributed On-Chip Rectifier

- Exploits rectifier portion of buck converter
  - Generates and distributes power supplies in 3-D integrated circuits
  - Eliminates need for on-chip inductors
- Rectifier is composed of transmission lines
  - Terminated with lumped capacitances
- Inter-plane structure is connected by 3-D TSVs
- Low pass behavior
  - $RC$-like characteristics
  - Sharp roll-off
  - Due to distributed nature

Schematic Structure of the 3-D Rectifier

Physical Layout of Distributed Rectifier

Plane C (upper)  Plane B (middle)  Plane A (bottom)

On-chip capacitors  On-chip capacitors  On-chip capacitors

Interconnects  Ring oscillators and buffers  Switched current loads

Power supply noise measurement
Power Delivery Test Circuit

- Lincoln Lab 3-D CMOS process
  - 150 nm FDSOI
  - Three physical planes
  - Three metal layers per plane
  - Back side metal on top two planes
  - Each wafer is separately processed

On-Chip Integration of Voltage Converters

- Simultaneous decap placement with distributed power supplies
- Active filter regulators as distributed power supplies
- On-chip converters
  - Simultaneous voltage regulator and decap placement in a multi-plane structure
  - Increased complexity
  - Local voltage generation close to load (point-of-load)
  - Lower P/G noise among at the power distribution network
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Tezzaron: 3-D Logic on Memory
Multi-Project Wafer (MPW)

• Two logic layers
  – 130 nm process
  – Six metal levels per plane
    • Five metals for interconnect
    • Metal 6 for face-to-face bonding
  – 5 x 5 mm²
  – Wafer-to-wafer bonded
• One DRAM controller layer
  – ~ 800 I/O pads for communication with outside world
• Two layers DRAM cells
  – Proprietary technology
  – 1 Gbit data per plane
• Logic bonded to memory by die-to-wafer process
Next 3-D Test Circuit Projects
Tezzaron Logic Planes

• 3-D free optical system
  – VCSEL driver circuitry (transmitter)
  – Transimpedance amplifier (receiver)
  – Limiting amplifier (receiver)
    • Volt to volt converter
  – Distributed pulse generation circuitry
  – Injection locked clock multiplier

• 3-D microprocessor
  – Bit-error-rate at different stages of pipeline
  – Cross-plane thermal stressing

• Decap placement in 3-D stack
  – Noise generating circuits
  – $V_{dd}$ and $G_{nd}$ noise detect circuits

• Thermal aware floorplanning
  – Cross-plane thermal coupling
  – Heat generators
  – On-chip thermal sensors

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Hybrid Optical 3-D NoC

3-D Free Space Optics

Dedicated transmitters
- \( N^2 \) lasers
- Simple, fast (no WDM)
- Area = 5 mm\(^2\) for 16 node system
- Consumes energy only when "ON"

Shared receivers
- No dedicated receivers needed

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Design Methodologies for Heterogeneous 3-D Integrated Systems

- Integrate processing and sensing within a multi-plane system
- Develop design methodologies to manage plane-to-plane interactions
  - Prevent processing planes from disturbing sensor planes
- Develop general purpose processing planes
  - Compatible with
    - Different types of sensors
    - Disparate communication schemes
- Manage heterogeneous data fusion
Conclusions

• Three-dimensional integration is a promising solution to expected limits of scaling
• Interplane through silicon vias (TSVs) are the key technology
• Advanced and novel 3-D architectures are now possible
• We've demonstrated a 3-D test circuit operating at 1.4 GHz
  – 3-D power delivery test circuit currently being fabricated
  – Multiple 3-D circuits currently being designed
  – More to come from many sources

• 3-D integration is a likely next step in the evolution of semiconductor technology

Thank you for your attention!