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Josephson Junction Digital Circuits -- Challenges and Opportunities

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§ 1. Introduction

In spite of the rather large investment in research in superconducting electronics in the U.S. and Japan and elsewhere, there has been remarkably little payoff in terms of practical applications. By "practical applications" I mean products which are used by others outside the superconducting electronics community for their own purposes, without a primary interest in how the superconducting device works. By "electronics" I mean active electron devices, excluding passive conductors, filters, etc.

In fact I can think of only three successful examples. The first is the widely used SQUID magnetometer [1]. A second example is the SIS mixer [2] which is now deployed at every millimeter wavelength astronomy telescope. The third example is the Josephson voltage standard [3,4]. In the near future it seems likely that the superconducting hot-electron bolometer will join this list [5].

Note that these are all analog devices. There have been no successful digital applications of Josephson junctions. I believe there are two primary reasons for this. The first is integration scale. Each device on my list is really quite simple. Each requires only one or a few Josephson junctions, except for the voltage standard which requires only a single long series array of uniform junctions. Even the most elementary digital circuit, however, will be much more complex than this if it is to serve a useful function. It will require many Josephson junctions with well-controlled properties, with complex interconnections. This complexity puts great demands on fabrication tolerances. Given the comparatively primitive state of superconducting integrated circuit fabrication facilities, it is difficult to make a large complex digital circuit work reliably.

The second reason is the competition from other technologies. Each of the three analog devices on my "success" list is far superior to any competing technology because each relies on some fundamental property of superconductors: magnetic flux quantization provides an extremely precise measurement of magnetic field; the divergent density of states at the superconducting energy gap allows vanishing dark current in the SIS mixer; and the Josephson relations equate voltages to very accurate frequency standards. Superconducting digital circuits on the other hand are confronted by the astonishing and continuing progress of the established and extremely sophisticated technology of semiconductor integrated circuits. It will not be enough to merely surpass silicon and GaAs technology in performance. A successful superconducting digital circuit must provide a function vital enough to compensate for the much higher cost in time, money, and reliability which is inevitable in an immature technology.

Nevertheless, I am quite confident that the situation is changing, that we are at the beginning of a rebirth of superconducting digital electronics. This report will emphasize the prospects and the requirements for establishing this technology outside the superconducting electronics community. I will not attempt a general survey of the field, but will concentrate upon what I think are the most promising prospective applications of superconducting digital electronics in both the next few years and in the future, and on some more speculative but fascinating long term possibilities on an extremely large scale.

§ 2. Flux logic vs. voltage-state logic

All Josephson junction logic schemes can be roughly classified as either flux-based (SFQ) or voltage-based. I would like to discuss the relative merits of these two approaches in some detail, because it is my contention that the emphasis on voltage-state logic in the past -- most notably the IBM project ending in 1983 and the MITI project in the 1980's -- has been an unfortunate choice, and that this history has continuing regrettable consequences today.

Voltage-state Logic

Voltage-state logic is a natural emulation of semiconductor technology in that data is encoded by steady voltage levels. This is a very significant advantage. Since Josephson junction voltage-state logic resembles semiconductor logic, the entire and elaborate edifice of digital circuit design tools and concepts used for semiconductor integrated circuits can be rather directly applied to develop superconducting circuits. The design infrastructure for SFQ logic is much less well-developed, although the semiconductor experience is still highly relevant.

The long effort which has gone to Josephson junction voltage-state logic has led to impressive accomplishments. There are many examples of ~ 20,000 junction circuits which have been demonstrated, in comparison to the few ~ 2,000 junction circuits which have been demonstrated in SFQ logic. It should be noted however that the voltage-based demonstrations have been at several Gbps, compared to ~ 10 Gbps for the SFQ circuits.

The most crucial difference between these approaches is that voltage-state logic has an intrinsic maximum speed that is very much less than that of SFQ logics. Although complex SFQ logic circuits should be capable of 100 Gbps or more, a Josephson junction voltage-state logic cannot operate faster than a few Gbps. The speed might be increased to as much as 10 Gbps but with considerable error rate. This is just not fast enough. Complex semiconductor LSI circuits are now clocked as high as 10 Gbps (an example is a PRBS generator consisting of 2600 transistors [6]).

The maximum speed errors of voltage-state logic have generally been called "punchthrough," in analogy with certain errors in transistor operation. This name gives the impression that these errors are due to the device structure and hence could be eliminated with better technology. This is false. In fact, the errors are caused by the

fundamental topology of the phase space of a Josephson junction, and so are intrinsic in the standard voltage-state logic.

In effect, the maximum speed limitation of Josephson junction voltage-state logic arises because the fundamental parameters for the Josephson effect are I and f (the junction phase), not I and V. The Josephson equation $V = (\hbar/2e)\, df/dt$ states that if the voltage is constant the phase is increasing rapidly -- it is essentially undefined in the voltage state. The Josephson equation $I_b = I_c \sin f$ states that the phase must be well-defined in the zero-voltage state. Therefore in order to reset a Josephson junction from finite voltage to zero voltage the phase must be "recaptured."

Imagine some specified reset operation which is intended to take a junction from the voltage state to the zero voltage state, perhaps a prescribed current waveform as a function of time. Whatever this operation is, it must begin with a randomly distributed initial phase in the voltage state and end with some desired recapture phase f_0 which gives the desired current at zero voltage. Note however that the phase is unique only in the range [0,2ð]. This means that the recapture phase $f_0 + 2ð$ is completely equivalent to the recapture phase f_0. If the reset operation takes the initial phase f_i into the recapture phase f_0, it must also take the initial phase $f_i + 2ð$ into the recapture phase $f_0 + 2ð$. But what if the initial phase lies between f_i and $f_i + 2ð$? For any specific reset operation there must be some boundary between those initial phases evolving to f_0 and those initial phases evolving to $f_0 + 2ð$. If the initial phase happens to lie precisely on this boundary it will never decide between the two; it will sit at this metastable point. If it lies near the boundary it will take a long time to decide. If it takes too long, then a bit error occurs.

We can use this picture to calculate the minimum error rate of voltage-state logic as a function of operating speed. This is done in the Appendix. The conclusion is that the bit error rate due to phase recapture is too large for an integrated circuit operating at 10 GHz.

This picture also suggests a new kind of Josephson junction voltage-state logic which should be able to operate at much higher speed. If the Josephson junction never has to enter the zero-voltage supercurrent state these phase recapture errors cannot occur. In the standard convention, logic value "0" is represented by a Josephson junction at zero voltage, on its critical current; logic value "1" is represented by the junction near the gap voltage $+V_g$. If however a logic is designed so that "0" is represented by some other non-zero voltage, the phase need never be recaptured. This would eliminate the "punch-through" type of error which limits the speed, and thus enable the circuit to operate as fast as SFQ circuits. Perhaps the most straightforward choice is to represent logic value "0" by the Josephson junction at the negative gap voltage $-V_g$. I would call this V_+V_- logic. As an extra bonus, the chip could be subjected to a dc magnetic field to ensure that the zero-voltage state was not accessible, and flux-trapping could not be a problem because the Josephson effect does not play a role.

V_+V_- logic stands in the same relationship to standard voltage-state logic as the SIS mixer to the Josephson mixer. For many years many scientists attempted to use the Josephson effect for the sensitive detection of millimeter wavelength radiation. Progress was very slow; in some sense the problem was that the Josephson nonlinearity is *too*

nonlinear, and difficult to control (if the junction is not embedded in a SQUID loop). The SIS mixer operates on a different principle entirely, using only the quasiparticle nonlinearity of a Josephson junction and not the Josephson equations. SIS mixers very quickly gained practical and widespread success. Further details of this story can be found in [2].

I am suggesting a Josephson junction voltage-state logic which uses only the quasiparticle nonlinearity of the Josephson junction, the same nonlinearity as the SIS mixer. Perhaps the success of V_+V_- logic could be as great. I am not aware of any research in this direction.

RSFQ Logic

There is no better introduction to the principles and operation of RSFQ (Rapid Single Flux Quantum) logic than the seminal review by Likharev and Semenov [7]. I will repeat only a little of that information here.

RSFQ circuits consist almost entirely of interconnected SQUID loops, each including an inductance and two or more resistively shunted Josephson junctions. Single magnetic flux quanta (SFQ's) represent the data bits for computation. An SFQ can be stored in a SQUID loop and can be transferred between loops. When a bit is transferred it is accompanied by an "SFQ" voltage pulse of quantized size:

$$V(t)\,dt = \Phi_0 = h/2e = 2.07\ \text{mV}\bullet\text{ps}\ . \qquad (1)$$

Thus information is coded in an intrinsically digital object, whose magnitude is given by fundamental constants.

It is convenient to represent each Josephson junction by its *Josephson inductance*. Using the Josephson equations

$$I_b = I_c \sin f \qquad V = \frac{h}{2e}\frac{df}{dt}\ , \qquad (2)$$

and the Faraday Induction Law $V = d\Phi/dt = d(LI)/dt$, where Φ is the magnetic flux, it is easy to see that the current-voltage relation for the Josephson effect has the form appropriate for an inductor which has a "Josephson inductance" which is equal to

$$L_J = L_{J0}\frac{f}{\sin f}\ , \qquad L_{J0} = \frac{h}{2eI_c}\ . \qquad (3)$$

Strange to say, this form never appears in the literature! (For more detail see [8].) It was in fact used in the theory of the Josephson parametric amplifier [9,10], but to my knowledge nowhere else. Rather, the much more familiar *incremental* Josephson inductance $h/2eI_c\cos f$ is very widely used, even where it is not proper to do so. It is instructive to graph these two expressions, as in Fig. 1. Note that the incremental Josephson inductance is a rather rapid function of the bias current and actually goes infinite when I_b approaches I_c. The real Josephson inductance is much better behaved,

almost flat, rising to a maximum of only ð/2 at $I_b = I_c$. To first approximation its current dependence can be ignored.

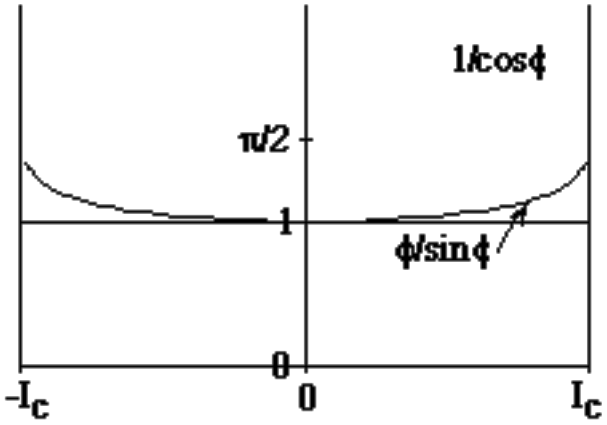

Fig. 1. The Josephson inductance and the incremental Josephson inductance are plotted.

This picture can be very helpful for the intuitive understanding of superconducting circuits. For instance, consider the "effective" magnetic flux in a SQUID loop, defined $_i L_i I_i$ where L_i represents all of the inductors including the Josephson inductors around the loop and I_i represents the dc current through each, with proper sign. This effective flux is an integer, $n\Phi_0$, in any SQUID loop. Roughly speaking, the inductors in RSFQ circuits are of two different values. If LI_c is, say, 1.5 Φ_0 then the SQUID loop can store a flux. If LI_c is, say, 0.5 Φ_0 then the SQUID loop will quickly transmit a flux which enters. In terms of the Josephson inductance one can say $L \quad 10 L_J$ for a storage loop and $L \quad 3 L_J$ for a transmission-line loop.

A most important consideration in the design of RSFQ circuits is how the dc bias current divides among the circuit elements. These currents avoid the resistors and only flow through the inductors and the Josephson junctions. A bias current into any network of inductors and Josephson junctions will divide exactly like the current into a resistive network, but with the R's replaced by L's. Therefore it is convenient to picture the operation of any RSFQ circuit starting from this constant dc bias current division, and then including additional integer flux quanta and the transient effects in the network superimposed.

§ 3. The challenge of circuit fabrication

In order to appreciate the parameters appropriate for RSFQ circuits, let us consider the SFQ pulse. Equation (1) relates the height V_{max} and width τ of an SFQ pulse, roughly $V_{max}\,\tau = \Phi_0$. The width τ is a very important parameter for RSFQ circuits. The fastest RSFQ gates are limited in speed by the requirement that the clock and data SFQ pulses arriving at the gate have independent effects. This means that the maximum clock frequency is somewhat less than $1/2\tau$. It is a general rule that maximum intrinsic circuit speed scales with $1/\tau$.

How large is τ? It is possible to derive an analytic expression from the resistively shunted junction equation if there is no capacitance. The time dependent voltage across a Josephson element shunted by resistance R, dc biased at $I_b > I_c$, can be written [11]

$$v(\theta) = \frac{\omega^2}{i - \cos \omega\theta} \tag{4}$$

in reduced units, with $i = I_b/I_c$, $\omega^2 = i^2 - 1$, the voltage v normalized by I_cR, and the time θ normalized by $h/2eI_cR$. If i is only slightly greater than unity, the voltage Eq. 4 consists of a series of isolated pulses with maximum voltage $v_{max} = i + 1$ 2. The full width at half maximum of each pulse is exactly two time units. In real units, the maximum voltage of the SFQ pulse is $V_{max} = 2I_cR$ and its width is $\tau = h/eI_cR$. The product of these is $\Phi_0 \bullet 2/\eth$, somewhat less than Φ_0 because of the long tails of the pulse. In this model it would be advantageous to make R as large as possible to maximize the circuit speed.

In reality, the $Nb/Al_2O_3/Nb$ Josephson junctions used for RSFQ circuits today do have shunt capacitance. This limits the largest R which can be used. R is generally chosen to make the parameter

$$\beta_c = 2eI_cR^2C/h \quad 1 . \tag{5}$$

This gives a quality factor Q = 1 for the L_JRC circuit constituting the Josephson junction (L_J is the Josephson inductance) and thus damps the "plasma oscillation" of this L_JC circuit. For real junctions with capacitance, $V_{max}\,\tau = \Phi_0$ is in fact appropriate. Today's RSFQ circuits generally have τ 5 ps, which implies a maximum clock frequency approaching $1/2\tau$ = 100 GHz. In order to decrease τ further it will be necessary to decrease C, and since $Nb/Al_2O_3/Nb$ junctions have specific capacitance 50 fF/μm ^{2} [12] this will require smaller junction area.

In most RSFQ circuits today the parameters used are: minimum junction area (3.5 μm)^2 and critical current density j_c 1000 A/cm ^{2}, implying I_c ε 100 μA. This I_c is appropriate both in that it gives a convenient inductor size, and that the Josephson junction coupling energy is enough larger than the thermal energy to allow a low bit-error rate. In the future it should be possible to make smaller high-j_c Josephson junctions for RSFQ circuits. Ultimately it would be desirable to use junctions with area (0.3 μm)^2 and j_c approaching 100,000 A/cm^2. Such lithography is not difficult for a modern semiconductor fabrication facility. The reduction of the minimum feature size by a factor of 10 will allow the circuit density to increase by much more than a factor of 100 (inductances can be scaled appropriately). This is because with such a small capacitance the SFQ pulse will be damped by the intrinsic normal-state resistance of the junction, and no external shunts are needed. The great increase in density will be required for RSFQ circuits if ULSI applications such as petaflops computing discussed below are ever to become a reality.

So far this discussion has been rather theoretical and a note of reality is needed. Even today, smaller, higher-j_c Josephson junctions with very high quality are quite common. The SIS mixer, an application much more demanding in terms of junction quality, often uses junctions with 10x smaller area and 10x larger j_c than just mentioned. But these

junctions are not used for RSFQ circuits. The crucial consideration is parameter control during fabrication. The conditions for small area, high j_C, high quality Josephson junctions on the one hand, and reproducible, high yield, well specified Josephson junctions on the other hand, do not generally coexist on the same fabrication line.

I believe that the quality of fabrication available today is the limiting factor, limiting for the speed, the integration scale, and the reliability of RSFQ circuits. The main problem is the fabrication-induced parameter variations, the differences between design and chip. For instance, it is common that if the circuits on one chip function correctly, the same circuits on a nominally identical chip may fail. More precisely, it is possible to use the fastest RSFQ gates to design complex circuits that will operate up to 90 GHz in simulation, using the nominal parameter values which can be specified under today's foundry design rules. This accords with the rough estimate above. However, when the expected 3σ design-to-chip parameter variations are included in the analysis, the maximum clock rate falls to slightly over 20 GHz [13]. The problem is not the failure of individual gates; RSFQ gates are designed to be very robust by using circuit optimization routines (such as that described in [14]). Rather it is the synchronization of the gates, the "timing," that causes the circuit to fail.

It is important to note that while the variations in Josephson junction area and j_C have long been a concern, on careful analysis these are much less important than the variations in resistance and inductance [15]. It is because the variations in the junctions' critical currents can be partially compensated by changing the bias current of the entire circuit. The importance of resistance and inductance is generally not appreciated because they hardly contribute to the failure of individual gates. In other words, an RSFQ gate with a deviant value of inductance or resistance is likely to give the correct output, but at the wrong time. This leads to the counterintuitive assertion that making smaller, high-j_C Josephson junctions will in itself not serve towards any improvement in large-scale RSFQ circuits. However, an improvement in fabrication control of resistance and inductance will have immediate benefit for the speed and reliability of practical RSFQ circuits.

§ 4. Synchronization

As RSFQ logic matures and larger circuits are built, more attention must be paid to architectural issues. This follows the history of semiconductor digital circuits. It is not generally appreciated how well-suited RSFQ circuits are to a variety of novel timing schemes which might allow ultra-high-speed digital operation. This is because timing signals in SFQ circuits are SFQ pulses as well, which travel through the circuit in the same way as the data SFQ's. It is not at all clear which clocking scheme will prevail as the most beneficial. A recent review of timing of RSFQ circuits is found in [16]. In this area RSFQ circuit design is leading semiconductors, which still almost completely emphasize equipotential zero-skew clocking, in the drive to learn how to coordinate the operations of a digital circuit on a picosecond timescale.

Most RSFQ circuits are synchronous and employ either counterflow clocking, in which the clock is distributed in the direction opposite to the data flow (positive clock

skew), or concurrent clocking, in which the clock is distributed in the same direction as the data flow (negative clock skew), or some combination of the two. Clock skew is defined as the difference between the times at which the clock signal arrives at two adjacent clocked cells. Evidently, the sum of the clock skews around a closed data loop must be zero, and this extra constraint is perhaps the reason why progress towards RSFQ circuits with a "recurrent" data path has been negligible compared with signal processing circuits with a regular systolic architecture.

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Fig. 2. Block diagram of a 64-bit circular shift register. The circuit was designed with careful allocation of clock skew around the data path.

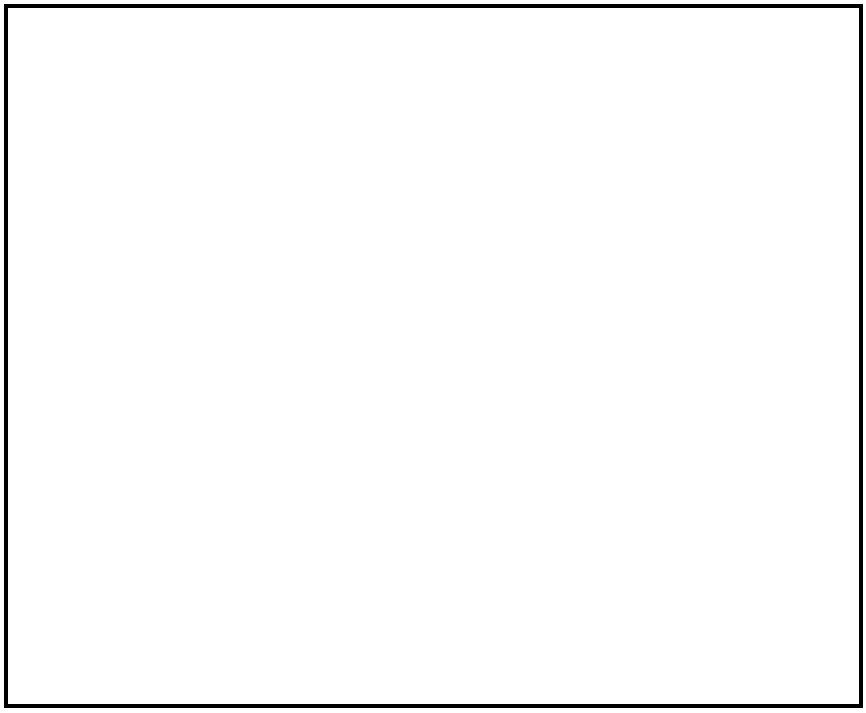

Fig. 3. Bias margins for correct operation during 200 ms for the 64-bit circular shift register, as a function of clock frequency.

To demonstrate the importance of design with special attention to timing constraints, we at Rochester focused on the simplest RSFQ recurrent circuit, the circular shift register (CSR). We designed three different 64-bit CSR's with distinct timing schemes [17]. The most successful to date is shown in Fig. 2. It operated properly up to a maximum clock frequency of 18.2 GHz, as seen in Fig. 3 [18]. This is quite close to the maximum *theoretical* clock frequency of 21 GHz for this circuit. Previously, the longest recurrent data path demonstrated in an RSFQ circuit was only a few stages long, and only operated to less than 4 GHz [19].

§ 5. Likely near-term applications

I believe that there must be small-scale applications of superconducting digital electronics before large-scale applications can exist. Such small-scale "stepping-stone" applications build up the infrastructure of the field, in manpower, techniques, fabrication facilities, etc. A successful stepping-stone application would provide legitimacy in the sense that it would prove to any doubters that this is a viable technology for at least some purposes. And it would provide experience in any technical problems which might not yet be appreciated. For these reasons any successful application however small-scale will be an enormous benefit to the entire research field.

Let me consider the attributes that will contribute towards a real-world practical application of superconducting digital electronics in the near future:

1. The RSFQ circuit should be simple, not complex. This means either a fairly small circuit, or a very repetitive circuit. The reason is that more complex circuits are much more troublesome to realize.

2. The RSFQ circuit must be able to be fabricated with today's fabrication technology.

3. It should be suitable for a single chip, because nobody has yet demonstrated the ability to pass SFQ pulses from chip to chip.

4. It should require a low output rate, to be compatible with laboratory instruments.

5. It is a great advantage if the application already provides a cryogenic environment.

6. Somebody else must need it very badly, or they will not choose to undergo the problems which are inevitable in introducing a new technology. This implies that the superconducting digital system provides a function considerably beyond competing technology.

I will describe three likely real-world digital applications of superconductivity which appear to fulfill these requirements. The first is the RSFQ time-to-digital converter (TDC) to be used in the instrumentation for particle physics colliders. The second is an SIS receiver with integrated RSFQ autocorrelator. The third possibility is the superconducting analog-to-digital converter (ADC) with some decimating circuitry.

Time-to-Digital Converter

In particle physics experiments the energy and mass of the reaction products of high-energy particle collisions must be determined as precisely as possible. The standard way to do this is to measure the time-of-flight of the created particles. This requires a very accurate measurement of the particle hit time for each particle detector channel. The time-to-digital converter (TDC) is a critical component to accomplish this.

Currently, the output from the cryogenic particle detectors is generally digitized at room temperature using semiconductor TDC's which dissipate too much heat to cool. This is unsatisfactory in that the low-heat-leak cables have narrow bandwidth, and they add noise to the low-level detector signal. A superconducting TDC and readout electronics would be located inside the detector cryostat and so avoid this problem.

The function of the TDC is simple and can be realized by very robust RSFQ circuits. Basically, the RSFQ TDC [20,21] counts the ticks of a high-speed clock between a system start signal and the detector hit signal. The counter is a simple chain of toggle flip-flops. The time resolution is equal to the clock period. A time resolution of 10 ps should be possible with current fabrication technology, along with the low power, linearity, multi-hit capability, and every other requirement for particle physics instrumentation.

Future colliders such as the LHC plan to have detectors with hundreds of thousands of channels. If it is necessary to use semiconductor timing and readout electronics for these detectors, this will require a severe compromise between power dissipation and performance and will be an important limitation to the utility of the entire accelerator.

Integrated SIS Receiver

The standard design of heterodyne receivers for millimeter-wavelength astronomy consists of an externally pumped SIS mixer followed by an isolator, a cooled HEMT IF amplifier, room-temperature postamplifiers, an ADC, and some spectrometer. The spectrometer of choice today is the digital autocorrelator. (A single channel of an autocorrelator multiplies the input signal by a delayed copy of that input signal. Multiple channels with multiple delays (or "lags") are needed to produce the entire spectrum.) This scheme has been very successful [2,22], but it has several deficiencies in information throughput. Almost all SIS receivers are single-pixel devices, with an instantaneous bandwidth of only 1 GHz. This is not due to the SIS mixers themselves, which are readily multiplexed and which are capable of 20% to 30% fractional bandwidth [23]. Rather, it is largely because multichannel spectrometers are complex and expensive.

It should be possible to remove these constraints on SIS receivers by using a superconducting back-end. The SIS mixer output could be directly digitized by a superconductor ADC and then fed to an RSFQ autocorrelator. A sketch of such a scheme is shown in Fig. 4. The superconducting back-end has the advantage that the digitization and autocorrelation could be performed at a very high clock rate, allowing a very high IF bandwidth. It would also allow large focal plane array SIS receivers to be constructed -- a 10 x 10 pixel SIS receiver could be housed in a standard 1 W cryostat.

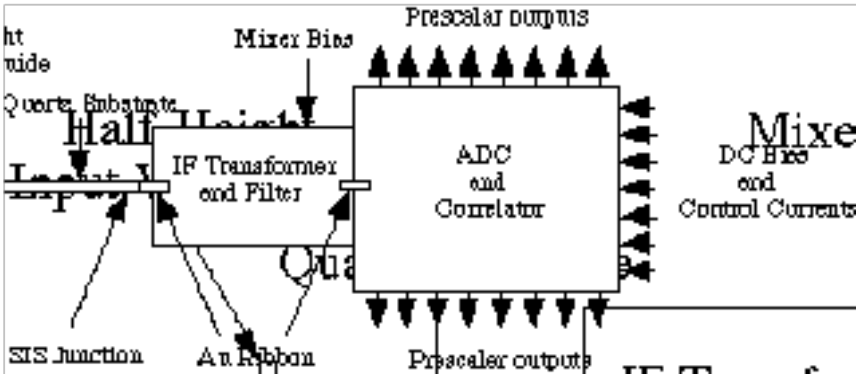

Fig. 4. Sketch of an integrated all-superconductor SIS mixer/back-end.

During the past few years there have been a number of proposals advanced for RSFQ digital correlators. These have converged to a one-bit design with double-Nyquist sampling [24],[25], which was developed for semiconductor correlators [26]. The *sign* of the input signal is represented by the binary {0,1} and multiplication is then simply the XOR operation. The accuracy lost by the one-bit digitization is partially compensated by the oversampling [27]. Experimental results have been impressive [28].

Here are some problems of this scheme. It will be difficult to match the low noise performance of semiconductor amplifiers; InP HEMT amplifiers can achieve $T_n(K) \approx f(GHz)/2$ in the laboratory [29]. The microwave engineering required to replace the function of the isolator will be difficult. But the most severe concern is the impracticality of high-speed multi-chip SFQ circuits in the near future.

With current fabrication technology, it appears that up to 256 lags can fit on a 1 cm superconducting chip. The simplest correlators used in radio astronomy have 1024 lags, providing a 1 GHz spectrum in 1 MHz resolution bins. That resolution is important, because it is needed to resolve the spectral lines of interstellar molecules. Thus a single-chip RSFQ autocorrelator with 1 MHz resolution could provide only 256 MHz bandwidth, far from competitive unless it were part of a very large focal plane array.

However there are important astronomical objects which have very broad lines because they are very hot. Consider the possibility of a 650 GHz SIS receiver integrated with a one-bit superconducting ADC double-Nyquist sampled at 64 GHz and a 256 lag RSFQ autocorrelator, implying a frequency resolution of 62.5 MHz over a 16 GHz IF bandwidth. This would be an ideal instrument for searching for protogalaxies, very hot but distant young galaxies with unknown red-shift, most of which are likely to be invisible to the Hubble Space Telescope [30]. Such a project lies at the forefront of millimeter-wavelength astronomy.

Analog-to-Digital Converter

Superconducting ADC's have potential advantages over semiconductor devices in power, speed, dynamic range, and sensitivity. Because of this, superconducting ADC's have been the focus of much research for many years. Many designs with various

properties have been developed, each of which is well-suited for some applications and not for others. General discussions of Josephson ADC's are found in [31,32]. Since the data rate of these ADC's is so large, the circuitry often includes a decimation filter.

For example, a recent counting-type ADC employing 2100 Josephson junctions was tested successfully at a clock rate of 10.5 GHz, and showed 11 bits of resolution for an 8 MHz analog signal [33]. This is about comparable to the best semiconductor ADC's. Although this is probably the most remarkable demonstration of any complex RSFQ circuit to date, it is nevertheless quite a preliminary result, and along with other recent impressive experimental results it confirms the projected ability of single-flux-quantum ADC's of various design to deliver performance superior to any other technology.

Two important figures-of-merit for high-dynamic-range ADC's are the aperture time (the time required to sample the analog signal) and the jitter (the variation in time from one sample to the next), both of which should be small. In SFQ-based ADC's the aperture time is proportional to the width of an SFQ pulse, and so higher critical current density and smaller Josephson junction area should allow higher ADC performance. The low-noise environment of superconducting circuitry should enable low jitter, but research in this area is still rudimentary.

High-performance ADC's are important to many areas of science and technology. It is not at all clear when and where the advantages of superconducting ADC's will overcome the drawbacks of the developmental expense and unproven reliability. It is likely to come in an area where the analog signal is already at cryogenic temperatures, and there is an advantage to on-chip integration of a detector and digitizer. An example might be infrared focal-plane array detectors. It will however first require a clear-cut demonstration of superior performance compared to conventional semiconductor ADC's.

§ 6. Possible future applications

Once RSFQ circuits can be made on a larger integration scale, with more complex circuits on multiple chips connected through multi-chip modules (MCM's), wider possibilities will open. In my opinion the most likely future applications will fill the following requirements:

1. The RSFQ circuit should be not *too* complex, e.g. it should be much less intricate than a microprocessor.

2. The fabrication expense should be moderate, certainly requiring more sophistication in fabrication than available today but not a semiconductor-class dedicated billion dollar fabrication facility.

3. The RSFQ circuit should perform its function <u>much</u> better than competing technology.

4. And finally, the RSFQ circuit should replace a crucial subsystem or component of a large enterprise. This will give the user a strong incentive to facilitate development.

I will describe two applications which I believe fill these requirements. These are the digital correlator and more broadly, the area of digital signal processing.

Digital Correlators

Autocorrelation spectroscopy is widely used in radio astronomy to take a time series of a very small signal buried in noise and produce a time-averaged frequency spectrum. The autocorrelator for a modern single-dish telescope such as the Green Bank Telescope (GBT) consists of very many equipment shelves filled with VLSI semiconductor correlator chips, connected by intricate cabling. This is the current state-of-the-art.

Nevertheless much more correlation throughput could profitably be employed. A focal-plane array receiver with M independent pixels requires a multi-bank autocorrelator M times as large as the single-pixel receiver. Also there are a number of large multi-dish millimeter array observatories planned and in construction; to take full advantage of an N-dish array each baseline must be separately correlated, and so N(N-1)/2 times the correlator throughput is required compared to the single dish [34]. Therefore the correlators under design for future large arrays which will have 40, 50, or more dishes must push the current state-of-the-art, but must also make severe compromises. Although in principle any size correlator can be built with today's semiconductor technology by further multiplexing, the practical limitations are reliability, power dissipation, cost, and complexity of interconnections. The largest correlators today fall comfortably within these constraints, but not by a large margin. In this sense the correlator is now the limiting subsystem for radio astronomy instrumentation.

A large "hybrid" autocorrelator can provide a correlation bandwidth of perhaps 16 GHz using semiconductor chips with clock rate of only several hundred MHz. It does this by subdividing the input and taking the cross-correlation functions of all the subdivisions. This is why wide-bandwidth correlators are so complex. However, the complexity decreases as the *square* of the clock speed. This means that superconducting correlators compete with much more complex semiconductor correlators. Other features favorable to the implementation of RSFQ correlators are the cryogenic environment of the detectors, SIS mixers and others, operation without need to communicate to the (room temperature) external world except at low speed for the time-averaged spectrum, and their simple architecture compared to other large superconducting circuits.

The GBT correlator chips have figure of merit (number of lags x clock rate) F = 128 lag-GHz [35]. Superconducting correlator chips of this performance have already been demonstrated [28]. F values of ten or even a hundred times as large should be possible in the next few to ten years.

Digital Signal Processing

Digital Signal Processing (in contrast to general purpose computing) is a large and growing subset of digital circuitry. In many applications it is advantageous to perform repetitive computational processes, free of conditional branching statements, at the highest possible speed. In digital bandpass filtering, for one example, random access to memory is not necessary. Stored coefficients are called in sequence, predictably and unconditionally. The premium is on raw computational speed.

Because of this, much of the research on RSFQ logic has been directed toward various DSP functions. Some larger circuits are described in [36,37,38]. The attributes of DSP which favor RSFQ logic are regular circuit topology, a small number of distinct cells, limited interconnections, moderate output rate of the processed signal in many cases, and little memory requirement.

RSFQ logic might find its greatest utility in applications where large-scale real-time signal processing is required. Several of the possibilities considered have been multi-spectral observations, impulse coded radar, phased arrays, and high speed fiber-optic CDMA decoding. In each case, the signal processing speed of conventional technology has been a bottleneck to current or future system performance.

§ 7. Speculative large-scale applications

This section is a change of pace. In the above, evolutionary improvements upon demonstrated SFQ digital circuits may overtake established semiconductor technology, by capitalizing on the particular advantages of superconductivity. Here I will describe two more speculative ideas which, all will agree, are extremely difficult to accomplish with superconducting circuitry. They would require revolutionary technical advances and in particular a large improvement in superconductor circuit fabrication. But the objectives appear even much more difficult using conventional technology.

Petaflops-Scale Computing

A petaflops (10^{15} floating point operations per second) computer in any technology would require an enormous investment, but that investment is considered because petaflops marks a threshold where new kinds of computations will become practical for the first time [39]. Many believe that this can not be accomplished with future CMOS technology. One reason is that even very optimistic predictions for CMOS technology show clock rates of perhaps a few GHz for the foreseeable future [40]. A parallel-processing architecture capable of coping with the required parallelism of order 10^6 is not evident. Even more troublesome is the large power requirement for any semiconductor computer of this scale. The enormous flow of heat would require that the computer have a very large volume; and the estimated ~100-ns latency resulting from signal propagation over such distances would likely defeat any parallel processing architecture.

A large trial project has recently begun in the United States to explore the plausibility of petaflops computation based on RSFQ logic, under the title "Hybrid Technology Multi-threaded (HTMT) Architecture." Ref. [41] is a news article previewing the HTMT project. One HTMT specification projected 10,000 RSFQ processors, each providing 100 gigaflops. Each processor will consist of about 30 chips in a multi-chip module. Each 2 cm x 2 cm chip will have 4,000,000 Josephson junctions (0.8 μm linewidth with j_c = 20 kA/cm^2) and run at a clock speed of 100 GHz and dissipate 30 mW at 4 K. Most recent results and specifications are given in [42]. Other components of the HTMT system, such

as the holographic memory and the wideband optical interconnection network, are equally as visionary. This is a breathtakingly ambitious project.

Quantum Coherent Computation

Quantum coherent computation has drawn great interest in the press lately. Rather than using binary bits to encode data as in a conventional computer, quantum mechanical "qubits" can be in a coherent combination of "0" and "1." When a calculation is performed on a collection of such qubits, it explores the entire Hilbert space of all possible initial states. This so-called "quantum parallelism" explains the attraction of quantum coherent computation. Applications such as database search, factoring large numbers, and presumably many other NP problems can be solved in polynomial time on a hypothetical quantum computer. For a recent review see [43].

What technology could be used to build such a machine? One essential requirement is the capability to eventually fabricate a many-qubit network (at least thousands) with good parameter tolerance. Even though early demonstrations of coherent logic use microscopic systems, most agree that an integrated circuit technology will be necessary to reach an interesting level of complexity. Therefore more recent proposals have concentrated on solid-state systems including single electron devices and quantum dots.

But the most fundamental requirement for coherent computation is a long decoherence time for the qubit system, compared to the elementary operation time. Normal metal and semiconductor devices, including quantum dots, are unlikely to satisfy this, because they are strongly coupled to a large number of internal degrees of freedom, elastic vibrations, conduction electron excitations, etc., with a continuous energy spectrum, and so it is very difficult to isolate the qubit mode for very long. For example, a leading proposal for quantum dot qubits estimates decoherence times of a nanosecond compared to gate operations taking one thousand times longer [44]. Superconducting single electron devices, and indeed all electrically coupled solid-state devices, have a similar problem of isolation from substrate modes: coupling to high-frequency 1/f dielectric noise gives a maximum coherence time of order nanoseconds [45]. In fact, even "classical" single electron logic circuits fail (in simulation) for an induced charge $Q > 0.03$ e, much smaller than expected in any dielectric [46].

That leaves the superconductor magnetic flux quantum as the one best hope for useful quantum computation. Superconductors have extremely low entropy, a vanishing specific heat at low temperature, which implies very few available internal modes. In fact, in [47] it is estimated that a SQUID qubit may have a ratio of dephasing time to switching time of 10^{10} using future fabrication technology, a figure of merit which compares well with highly isolated atomic systems. SQUID qubits were intensively studied in the 1980's in another context, called "macroscopic quantum coherence" (see for instance [48]), although never demonstrated. Does Nature allow a quantum coherent two-state system on such a decidedly macroscopic scale?

If macroscopic quantum coherence can be attained in an rf SQUID, if the decoherence time is long enough, if a method to control the superposition state of the system (as "tipping" pulses) can be devised and demonstrated, then it would seem likely that a large-scale quantum computer could be made using superconductors. If all this would appear to be difficult to achieve, the difficulties are much much more severe in any other possibility for quantum coherent computation.

§ 8. Conclusion

There are many other candidates for future electronic systems, which promise to equal or exceed superconducting digital electronics in density and low power dissipation or in speed, sometimes enumerated as "nano-electronics" [49]. Many of these rely on physically interesting devices, and some may have great long-range potential. However, they are generally very different from established semiconductor technology in both structure and in operation. Therefore, they will require an enormous investment, both money and time, in fabrication technology and in computer architecture development before they can serve a useful function.

Superconducting digital electronics, in particular RSFQ logic, requires a much more modest investment. This is because it is actually quite close to established semiconductor technology in the following ways:

1. The fabrication is (almost) a subset of semiconductor circuit fabrication, although simpler.

2. Clocking is governed by the same rules and constraints as semiconductor circuits [16] and so the Boolean architectures extensively developed for today's universal semiconductor VLSI can be adapted for RSFQ.

Another advantage over nano-electronics is that RSFQ has gone through a kind of trial-by-fire, and it still survives. I mean that various problems which are irrelevant for single devices or small-scale circuits, but which would prevent integrated circuit development -- suggested show-stoppers such as interface to room-temperature electronics [50], deleterious effects of trapped flux [51], unforeseen error mechanisms [52], ultra-high-speed synchronization problems [16] -- are ever less daunting in the face of continuing progress. Now far from a hypothetical construct or a laboratory curiosity, RSFQ digital circuitry is on the verge of becoming an established technology.

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§ Appendix: Error Rate of Voltage-State Logic

The resistively shunted junction equation of a Josephson junction can be written:

$$i(t) = \sin f + \frac{\ddot{f}}{\omega_g} + \frac{\dot{f}}{\omega_{pl}^2} \qquad (6)$$

where i(t) is the applied current waveform as a function of time, normalized to the critical current I_c, $\omega_g = 2eI_cR/h$, and $\omega_{pl}^2 = 2eI_c/hC$. For specificity we assume i( ) = 0, although any other choice will serve as well. Let us examine the time evolution of f. Starting with any $f(0)$ and $\dot{f}(0)$, we know that $f( ) = 0$ (or 2π or …) with $\dot{f} = 0$ and $\ddot{f} = 0$. The exception is if the initial conditions lie on the metastable boundary -- call it $f_b(0), \dot{f}_b(0)$. In that case $f_b( ) = \pi$.

To calculate the error rate, we wish to determine the range of $f(0)$ for which $f(t^*)$ is still close to $f_b(t^*)$ after a long time t*, given the same i(t) and $\dot{f}(0)$. So let us take $f(t) = f_b(t) + \varepsilon(t)$, where $\varepsilon(0)$ is very small and $\dot{\varepsilon}(0) = 0$. Then Eq. 6 becomes

$$0 = \varepsilon \cos f_b + \frac{\ddot{f}}{\omega_g} + \frac{\ddot{\varepsilon}}{\omega_{pl}^2} \quad . \tag{7}$$

We are only interested in ε while it is still very small, i.e. while $f(t)$ is still very close to the metastable boundary. Once $f(t)$ moves away from the boundary its evolution becomes rapid and the Josephson junction soon settles into its stable point. Therefore we can ignore the $\ddot{f}$ term and Eq. 7 becomes

$$\ddot{\varepsilon} = -\varepsilon \omega_{pl}^2 \cos f_b \, . \tag{8}$$

ε grows most rapidly when $\cos f_b = -1$, so we choose that to get a <u>minimum</u> error rate. The solution of Eq. 8 is

$$\varepsilon(t \gg \omega_{pl}^{-1}) = \frac{\varepsilon(0)}{2} \, e^{\omega_{pl} t} \quad . \tag{9}$$

Let t* be the time allowed to reset a Josephson junction during a logic operation. Equation 9 says that a bit error occurs whenever $f(0)$ is roughly in the range $\pm 2 e^{-\omega_{pl} t^*}$ around $f_b(0)$. Since $f(0)$ is randomly distributed over a range of 2π, this means that the minimum bit error rate is

$$\text{BER} \quad \frac{2}{\pi} \, e^{-\omega_{pl} t^*} \quad . \tag{10}$$

A more careful calculation, and simulations of the error rate, agree with this [53]. If one-quarter of the clock period is allowed for reset, then Eq. 10 predicts an error rate of more than 10^{-9} per junction reset, with a 10 GHz clock rate and critical current density 1 kA/cm^2. This is much too large for an integrated circuit.

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