Texas Instruments

Op Amps For Everyone

Ron Mancini, Editor in Chief

Design Reference

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Chapter 1

The Op Amp's Place In The World

Ron Mancini

In 1934 Harry Black[1] commuted from his home in New York City to work at Bell Labs in New Jersey by way of a railroad/ferry. The ferry ride relaxed Harry enabling him to do some conceptual thinking. Harry had a tough problem to solve; when phone lines were extended long distances, they needed amplifiers, and undependable amplifiers limited phone service. First, initial tolerances on the gain were poor, but that problem was quickly solved with an adjustment. Second, even when an amplifier was adjusted correctly at the factory, the gain drifted so much during field operation that the volume was too low or the incoming speech was distorted.

Many attempts had been made to make a stable amplifier, but temperature changes and power supply voltage extremes experienced on phone lines caused uncontrollable gain drift. Passive components had much better drift characteristics than active components had, thus if an amplifier's gain could be made dependent on passive components, the problem would be solved. During one of his ferry trips, Harry's fertile brain conceived a novel solution for the amplifier problem, and he documented the solution while riding on the ferry.

The solution was to first build an amplifier that had more gain than the application required. Then some of the amplifier output signal was fed back to the input in a manner that makes the circuit gain (circuit is the amplifier and feedback components) dependent on the feedback circuit rather than the amplifier gain. Now the circuit gain is dependent on the passive feedback components rather than the active amplifier. This is called negative feedback, and it is the underlying operating principle for all modern day op amps. Harry had documented the first intentional feedback circuit during a ferry ride. I am sure unintentional feedback circuits had been built prior to that time, but the designers ignored the effect!

I can hear the squeals of anguish coming from the managers and amplifier designers. I imagine that they said something like this, "it is hard enough to achieve 30-kHz gain–bandwidth (GBW), and now this fool wants me to design an amplifier with 3-MHz GBW. But, he is still going to get a circuit gain GBW of 30 kHz". Well, time has proven Harry right, but there is a minor problem that Harry didn't discuss in detail, and that is the oscillation

problem. It seems that circuits designed with large open loop gains sometimes oscillate when the loop is closed. A lot of people investigated the instability effect, and it was pretty well understood in the 1940s, but solving stability problems involved long, tedious, and intricate calculations. Years passed without anybody making the problem solution simpler or more understandable.

In 1945 H. W. Bode presented a system for analyzing the stability of feedback systems by using graphical methods. Until this time, feedback analysis was done by multiplication and division, so calculation of transfer functions was a time consuming and laborious task. Remember, engineers did not have calculators or computers until the '70s. Bode presented a log technique that transformed the intensely mathematical process of calculating a feedback system's stability into graphical analysis that was simple and perceptive. Feedback system design was still complicated, but it no longer was an art dominated by a few electrical engineers kept in a small dark room. Any electrical engineer could use Bode's methods to find the stability of a feedback circuit, so the application of feedback to machines began to grow. There really wasn't much call for electronic feedback design until computers and transducers become of age.

The first real-time computer was the analog computer! This computer used preprogrammed equations and input data to calculate control actions. The programming was hard wired with a series of circuits that performed math operations on the data, and the hard wiring limitation eventually caused the declining popularity of the analog computer. The heart of the analog computer was a device called an operational amplifier because it could be configured to perform many mathematical operations such as multiplication, addition, subtraction, division, integration, and differentiation on the input signals. The name was shortened to the familiar *op amp*, as we have come to know and love them. The op amp used an amplifier with a large open loop gain, and when the loop was closed, the amplifier performed the mathematical operations dictated by the external passive components. This amplifier was very large because it was built with vacuum tubes and it required a high-voltage power supply, but it was the heart of the analog computer, thus its large size and huge power requirements were accepted as the price of doing business. Many early op amps were designed for analog computers, and it was soon found out that op amps had other uses and were very handy to have around the physics lab.

At this time general-purpose analog computers were found in universities and large company laboratories because they were critical to the research work done there. There was a parallel requirement for transducer signal conditioning in lab experiments, and op amps found their way into signal conditioning applications. As the signal conditioning applications expanded, the demand for op amps grew beyond the analog computer requirements, and even when the analog computers lost favor to digital computers, the op amp survived because of its importance in universal analog applications. Eventually digital computers replaced the analog computers (a sad day for real-time measurements), but the demand for op amps increased as measurement applications increased.

The first signal conditioning op amps were constructed with vacuum tubes prior to the introduction of transistors, so they were large and bulky. During the ’50s, miniature vacuum tubes that worked from lower voltage power supplies enabled the manufacture of op amps that shrunk to the size of a brick used in house construction, so the op amp modules were nicknamed *bricks*. Vacuum tube size and component size decreased until an op amp was shrunk to the size of a single octal vacuum tube. Transistors were commercially developed in the ’60s, and they further reduced op amp size to several cubic inches, but the nickname brick still held on. Now the nickname brick is attached to any electronic module that uses potting compound or non-integrated circuit (IC) packaging methods. Most of these early op amps were made for specific applications, so they were not necessarily general purpose. The early op amps served a specific purpose, but each manufacturer had different specifications and packages; hence, there was little second sourcing among the early op amps.

ICs were developed during the late 1950s and early 1960s, but it wasn’t till the middle 1960s that Fairchild released the μA709. This was the first commercially successful IC op amp, and Robert J. Widler designed it. The μA709 had its share of problems, but any competent analog engineer could use it, and it served in many different analog applications. The major drawback of the μA709 was stability; it required external compensation and a competent analog engineer to apply it. Also, the μA709 was quite sensitive because it had a habit of self destructing under any adverse condition. The self-destruction habit was so prevalent that one major military equipment manufacturer published a paper titled something like, *The 12 Pearl Harbor Conditions of the μA709*. The μA741 followed the μA709, and it is an internally compensated op amp that does not require external compensation if operated under data sheet conditions. Also, it is much more forgiving than the μA709. There has been a never-ending series of new op amps released each year since then, and their performance and reliability has improved to the point where present day op amps can be used for analog applications by anybody.

The IC op amp is here to stay; the latest generation op amps cover the frequency spectrum from 5-kHz GBW to beyond 1-GHz GBW. The supply voltage ranges from guaranteed operation at 0.9 V to absolute maximum voltage ratings of 1000 V. The input current and input offset voltage has fallen so low that customers have problems verifying the specifications during incoming inspection. The op amp has truly become the universal analog IC because it performs all analog tasks. It can function as a line driver, comparator (one bit A/D), amplifier, level shifter, oscillator, filter, signal conditioner, actuator driver, current source, voltage source, and many other applications. The designer’s problem is how to rapidly select the correct circuit/op amp combination and then, how to calculate the passive component values that yield the desired transfer function in the circuit.

This book deals with op amp circuits — not with the innards of op amps. It treats the calculations from the circuit level, and it doesn’t get bogged down in a myriad of detailed calculations. Rather, the reader can start at the level appropriate for them, and quickly move on to the advanced topics. If you are looking for material about the innards of op amps

you are looking in the wrong place. The op amp is treated as a completed component in this book.

The op amp will continue to be a vital component of analog design because it is such a fundamental component. Each generation of electronics equipment integrates more functions on silicon and takes more of the analog circuitry inside the IC. Don't fear, as digital applications increase, analog applications also increase because the predominant supply of data and interface applications are in the real world, and the real world is an analog world. Thus, each new generation of electronics equipment creates requirements for new analog circuits; hence, new generations of op amps are required to fulfill these requirements. Analog design, and op amp design, is a fundamental skill that will be required far into the future.

References

1 Black, H. S., *Stabilized Feedback Amplifiers*, BSTJ, Vol. 13, January 1934

Chapter 2

Review of Circuit Theory

Ron Mancini

2.1 Introduction

Although this book minimizes math, some algebra is germane to the understanding of analog electronics. Math and physics are presented here in the manner in which they are used later, so no practice exercises are given. For example, after the voltage divider rule is explained, it is used several times in the development of other concepts, and this usage constitutes practice.

Circuits are a mix of passive and active components. The components are arranged in a manner that enables them to perform some desired function. The resulting arrangement of components is called a circuit or sometimes a circuit configuration. The art portion of analog design is developing the circuit configuration. There are many published circuit configurations for almost any circuit task, thus all circuit designers need not be artists.

When the design has progressed to the point that a circuit exists, equations must be written to predict and analyze circuit performance. Textbooks are filled with rigorous methods for equation writing, and this review of circuit theory does not supplant those textbooks. But, a few equations are used so often that they should be memorized, and these equations are considered here.

There are almost as many ways to analyze a circuit as there are electronic engineers, and if the equations are written correctly, all methods yield the same answer. There are some simple ways to analyze the circuit without completing unnecessary calculations, and these methods are illustrated here.

2.2 Laws of Physics

Ohm's law is stated as V=IR, and it is fundamental to all electronics. Ohm's law can be applied to a single component, to any group of components, or to a complete circuit. When the current flowing through any portion of a circuit is known, the voltage dropped across that portion of the circuit is obtained by multiplying the current times the resistance (Equation 2–1).

$$V = IR \tag{2–1}$$

In Figure 2–1, Ohm's law is applied to the total circuit. The current, (I) flows through the total resistance (R), and the voltage (V) is dropped across R.

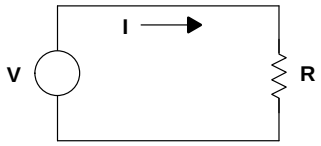


Figure 2–1. Ohm's Law Applied to the Total Circuit

In Figure 2–2, Ohm's law is applied to a single component. The current (I_R) flows through the resistor (R) and the voltage (V_R) is dropped across R. Notice, the same formula is used to calculate the voltage drop across R even though it is only a part of the circuit.

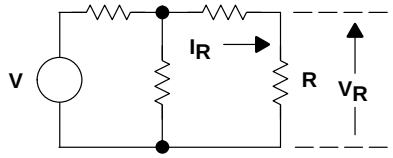


Figure 2–2. Ohm's Law Applied to a Component

Kirchoff's voltage law states that the sum of the voltage drops in a series circuit equals the sum of the voltage sources. Otherwise, the source (or sources) voltage must be dropped across the passive components. When taking sums keep in mind that the sum is an algebraic quantity. Kirchoff's voltage law is illustrated in Figure 2–3 and Equations 2–2 and 2–3.

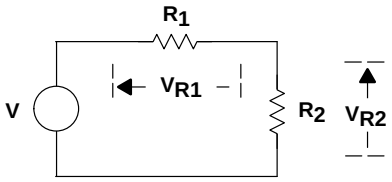


Figure 2–3. Kirchoff's Voltage Law

$$\sum V_{SOURCES} = \sum V_{DROPS} \tag{2–2}$$

$$V = V_{R1} + V_{R2} \tag{2–3}$$

Kirchoff's current law states: the sum of the currents entering a junction equals the sum of the currents leaving a junction. It makes no difference if a current flows from a current

source, through a component, or through a wire, because all currents are treated identically. Kirchoff's current law is illustrated in Figure 2–4 and Equations 2–4 and 2–5.

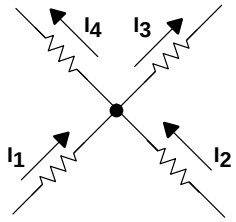


Figure 2–4. Kirchoff's Current Law

$$\sum I_{IN} = \sum I_{OUT} \tag{2–4}$$

$$I_1 + I_2 = I_3 + I_4 \tag{2–5}$$

2.3 Voltage Divider Rule

When the output of a circuit is not loaded, the voltage divider rule can be used to calculate the circuit's output voltage. Assume that the same current flows through all circuit elements (Figure 2–5). Equation 2–6 is written using Ohm's law as $V = I (R_1 + R_2)$. Equation 2–7 is written as Ohm's law across the output resistor.

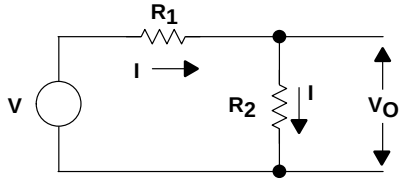


Figure 2–5. Voltage Divider Rule

$$I = \frac{V}{R_1 + R_2} \tag{2–6}$$

$$V_{OUT} = IR_2 \tag{2–7}$$

Substituting Equation 2–6 into Equation 2–7, and using algebraic manipulation yields Equation 2–8.

$$V_{OUT} = V \frac{R_2}{R_1 + R_2} \tag{2–8}$$

A simple way to remember the voltage divider rule is that the output resistor is divided by the total circuit resistance. This fraction is multiplied by the input voltage to obtain the out-

put voltage. Remember that the voltage divider rule always assumes that the output resistor is not loaded; the equation is not valid when the output resistor is loaded by a parallel component. Fortunately, most circuits following a voltage divider are input circuits, and input circuits are usually high resistance circuits. When a fixed load is in parallel with the output resistor, the equivalent parallel value comprised of the output resistor and loading resistor can be used in the voltage divider calculations with no error. Many people ignore the load resistor if it is ten times greater than the output resistor value, but this calculation can lead to a 10% error.

2.4 Current Divider Rule

When the output of a circuit is not loaded, the current divider rule can be used to calculate the current flow in the output branch circuit (R_2). The currents I_1 and I_2 in Figure 2–6 are assumed to be flowing in the branch circuits. Equation 2–9 is written with the aid of Kirchoff's current law. The circuit voltage is written in Equation 2–10 with the aid of Ohm's law. Combining Equations 2–9 and 2–10 yields Equation 2–11.

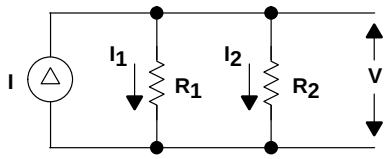


Figure 2–6. Current Divider Rule

$$I = I_1 + I_2 \tag{2–9}$$

$$V = I_1R_1 = I_2R_2 \tag{2–10}$$

$$I = I_1 + I_2 = I_2\frac{R_2}{R_1} + I_2 = I_2\left(\frac{R_1 + R_2}{R_1}\right) \tag{2–11}$$

Rearranging the terms in Equation 2–11 yields Equation 2–12.

$$I_2 = I\left(\frac{R_1}{R_1 + R_2}\right) \tag{2–12}$$

The total circuit current divides into two parts, and the resistance (R_1) divided by the total resistance determines how much current flows through R_2. An easy method of remembering the current divider rule is to remember the voltage divider rule. Then modify the voltage divider rule such that the opposite resistor is divided by the total resistance, and the fraction is multiplied by the input current to get the branch current.

2.5 Thevenin's Theorem

There are times when it is advantageous to isolate a part of the circuit to simplify the analysis of the isolated part of the circuit. Rather than write loop or node equations for the complete circuit, and solving them simultaneously, Thevenin's theorem enables us to isolate the part of the circuit we are interested in. We then replace the remaining circuit with a simple series equivalent circuit, thus Thevenin's theorem simplifies the analysis.

There are two theorems that do similar functions. The Thevenin theorem just described is the first, and the second is called Norton's theorem. Thevenin's theorem is used when the input source is a voltage source, and Norton's theorem is used when the input source is a current source. Norton's theorem is rarely used, so its explanation is left for the reader to dig out of a textbook if it is ever required.

The rules for Thevenin's theorem start with the component or part of the circuit being replaced. Referring to Figure 2–7, look back into the terminals (left from C and R_3 toward point XX in the figure) of the circuit being replaced. Calculate the no load voltage (V_{TH}) as seen from these terminals (use the voltage divider rule).

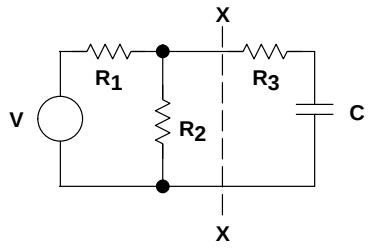


Figure 2–7. Original Circuit

Look into the terminals of the circuit being replaced, short independent voltage sources, and calculate the impedance between these terminals. The final step is to substitute the Thevenin equivalent circuit for the part you wanted to replace as shown in Figure 2–8.

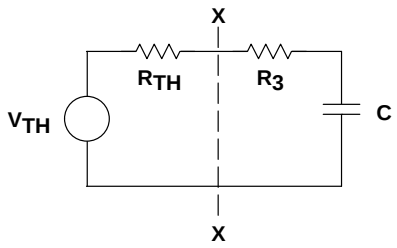
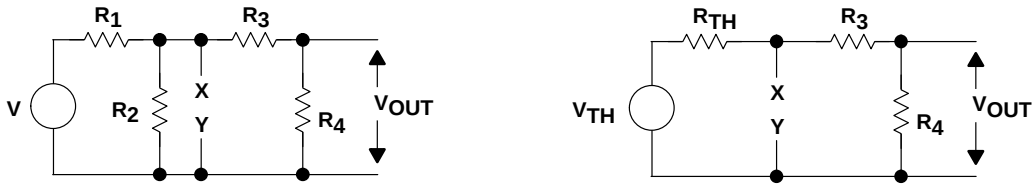


Figure 2–8. Thevenin's Equivalent Circuit for Figure 2–7

The Thevenin equivalent circuit is a simple series circuit, thus further calculations are simplified. The simplification of circuit calculations is often sufficient reason to use Thevenin's

theorem because it eliminates the need for solving several simultaneous equations. The detailed information about what happens in the circuit that was replaced is not available when using Thevenin's theorem, but that is no consequence because you had no interest in it.

As an example of Thevenin's theorem, let's calculate the output voltage (V_{OUT}) shown in Figure 2–9A. The first step is to stand on the terminals X–Y with your back to the output circuit, and calculate the open circuit voltage seen (V_{TH}). This is a perfect opportunity to use the voltage divider rule to obtain Equation 2–13.



(a) The Original Circuit **(b) The Thevenin Equivalent Circuit**

Figure 2–9. Example of Thevenin's Equivalent Circuit

$$V_{TH} = V \frac{R_2}{R_1 + R_2} \tag{2–13}$$

Still standing on the terminals X-Y, step two is to calculate the impedance seen looking into these terminals (short the voltage sources). The Thevenin impedance is the parallel impedance of R_1 and R_2 as calculated in Equation 2–14. Now get off the terminals X-Y before you damage them with your big feet. Step three replaces the circuit to the left of X-Y with the Thevenin equivalent circuit V_{TH} and R_{TH}.

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = R_1 \parallel R_2 \tag{2–14}$$

Note:

Two parallel vertical bars (||) are used to indicate parallel components as shown in Equation 2–14.

The final step is to calculate the output voltage. Notice the voltage divider rule is used again. Equation 2–15 describes the output voltage, and it comes out naturally in the form of a series of voltage dividers, which makes sense. That's another advantage of the voltage divider rule; the answers normally come out in a recognizable form rather than a jumble of coefficients and parameters.

$$V_{OUT} = V_{TH}\frac{R_4}{R_{TH} + R_3 + R_4} = V\left(\frac{R_2}{R_1 + R_2}\right)\frac{R_4}{\frac{R_1R_2}{R_1+R_2} + R_3 + R_4} \tag{2–15}$$

The circuit analysis is done the hard way in Figure 2–10, so you can see the advantage of using Thevenin's Theorem. Two loop currents, I_1 and I_2, are assigned to the circuit. Then the loop Equations 2–16 and 2–17 are written.

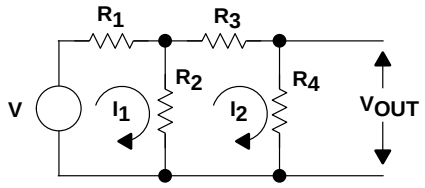


Figure 2–10. Analysis Done the Hard Way

$$V = I_1(R_1 + R_2) - I_2R_2 \tag{2–16}$$

$$I_2(R_2 + R_3 + R_4) = I_1R_2 \tag{2–17}$$

Equation 2–17 is rewritten as Equation 2–18 and substituted into Equation 2–16 to obtain Equation 2–19.

$$I_1 = I_2\frac{R_2 + R_3 + R_4}{R_2} \tag{2–18}$$

$$V = I_2\left(\frac{R_2 + R_3 + R_4}{R_2}\right)(R_1 + R_2) - I_2R_2 \tag{2–19}$$

The terms are rearranged in Equation 2–20. Ohm's law is used to write Equation 2–21, and the final substitutions are made in Equation 2–22.

$$I_2 = \frac{V}{\frac{R_2+R_3+R_4}{R_2}(R_1 + R_2) - R_2} \tag{2–20}$$

$$V_{OUT} = I_2R_4 \tag{2–21}$$

$$V_{OUT} = V\frac{R_4}{\frac{(R_2+R_3+R_4)(R_1+R_2)}{R_2} - R_2} \tag{2–22}$$

This is a lot of extra work for no gain. Also, the answer is not in a usable form because the voltage dividers are not recognizable, thus more algebra is required to get the answer into usable form.

2.6 Superposition

Superposition is a theorem that can be applied to any linear circuit. Essentially, when there are independent sources, the voltages and currents resulting from each source can be calculated separately, and the results are added algebraically. This simplifies the calculations because it eliminates the need to write a series of loop or node equations. An example is shown in Figure 2–11.

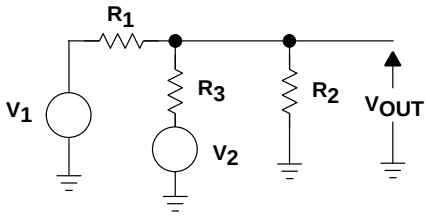


Figure 2–11. Superposition Example

When V_1 is grounded, V_2 forms a voltage divider with R_3 and the parallel combination of R_2 and R_1. The output voltage for this circuit (V_{OUT2}) is calculated with the aid of the voltage divider equation (2–23). The circuit is shown in Figure 2–12. The voltage divider rule yields the answer quickly.

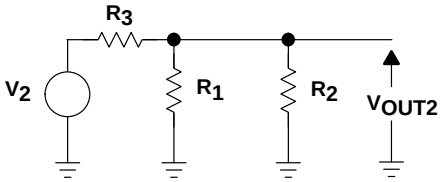


Figure 2–12. When V_1 is Grounded

$$V_{OUT2} = V_2 \frac{R_1 \parallel R_2}{R_3 + R_1 \parallel R_2} \tag{2–23}$$

Likewise, when V_2 is grounded (Figure 2–13), V_1 forms a voltage divider with R_1 and the parallel combination of R_3 and R_2, and the voltage divider theorem is applied again to calculate V_{OUT} (Equation 2–24).

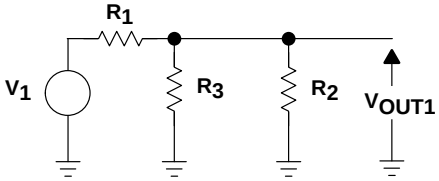


Figure 2–13. When V_2 is Grounded

$$V_{OUT1} = V_1 \frac{R_2 \parallel R_3}{R_1 + R_2 \parallel R_3} \tag{2–24}$$

After the calculations for each source are made the components are added to obtain the final solution (Equation 2–25).

$$V_{OUT} = V_1 \frac{R_2 \parallel R_3}{R_1 + R_2 \parallel R_3} + V_2 \frac{R_1 \parallel R_2}{R_3 + R_1 \parallel R_2} \tag{2–25}$$

The reader should analyze this circuit with loop or node equations to gain an appreciation for superposition. Again, the superposition results come out as a simple arrangement that is easy to understand. One looks at the final equation and it is obvious that if the sources are equal and opposite polarity, and when $R_1 = R_3$, then the output voltage is zero. Conclusions such as this are hard to make after the results of a loop or node analysis unless considerable effort is made to manipulate the final equation into symmetrical form.

2.7 Calculation of a Saturated Transistor Circuit

The circuit specifications are: when $V_{IN} = 12$ V, $V_{OUT} < 0.4$ V at $I_{SINK} < 10$ mA, and $V_{IN} < 0.05$ V, $V_{OUT} > 10$ V at $I_{OUT} = 1$ mA. The circuit diagram is shown in Figure 2–14.

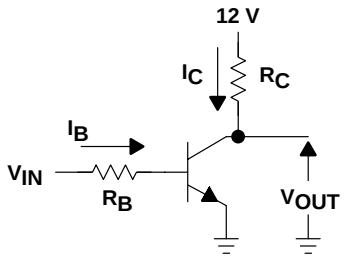


Figure 2–14. Saturated Transistor Circuit

The collector resistor must be sized (Equation 2–26) when the transistor is off, because it has to be small enough to allow the output current to flow through it without dropping more than two volts to meet the specification for a 10-V output.

$$R_C \leq \frac{V_{+12} - V_{OUT}}{I_{OUT}} = \frac{12 - 10}{1} = 2\ \text{k} \tag{2–26}$$

When the transistor is off, 1 mA can be drawn out of the collector resistor without pulling the collector or output voltage to less than ten volts (Equation 2–27). When the transistor is on, the base resistor must be sized (Equation 2–28) to enable the input signal to drive enough base current into the transistor to saturate it. The transistor beta is 50.

$$I_C = \beta I_B = \frac{V_{+12} - V_{CE}}{R_C} + I_L \approx \frac{V_{+12}}{R_C} + I_L \quad (2\text{–}27)$$

$$R_B \leq \frac{V_{IN} - V_{BE}}{I_B} \quad (2\text{–}28)$$

Substituting Equation 2–27 into Equation 2–28 yields Equation 2–29.

$$R_B \leq \frac{(V_{IN} - V_{BE})\beta}{I_C} = \frac{(12 - 0.6)50\ \text{V}}{\left[\frac{12}{2} + (10)\right]\text{mA}} = 35.6\ \text{k} \quad (2\text{–}29)$$

When the transistor goes on it sinks the load current, and it still goes into saturation. These calculations neglect some minor details, but they are in the 98% accuracy range.

2.8 Transistor Amplifier

The amplifier is an analog circuit (Figure 2–15), and the calculations, plus the points that must be considered during the design, are more complicated than for a saturated circuit. This extra complication leads people to say that analog design is harder than digital design (the saturated transistor is digital i.e.; on or off). Analog design is harder than digital design because the designer must account for all states in analog, whereas in digital only two states must be accounted for. The specifications for the amplifier are an ac voltage gain of four and a peak-to-peak signal swing of 4 volts.

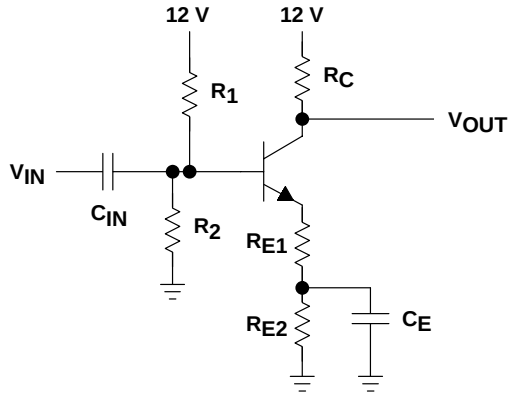


Figure 2–15. Transistor Amplifier

I_C is selected as 10 mA because the transistor has a current gain (β) of 100 at that point. The collector voltage is arbitrarily set at 8 V; when the collector voltage swings positive

2 V (from 8 V to 10 V) there is still enough voltage dropped across R_C to keep the transistor on. Set the collector-emitter voltage at 4 V; when the collector voltage swings negative 2 V (from 8 V to 6 V) the transistor still has 2 V across it, so it stays linear. This sets the emitter voltage (V_E) at 4 V.

$$R_C \leq \frac{V_{+12} - V_C}{I_C} = \frac{12\text{ V} - 8\text{ V}}{10\text{ mA}} = 400\ \Omega \tag{2–30}$$

$$R_E = R_{E1} + R_{E2} = \frac{V_E}{I_E} = \frac{V_E}{I_B + I_C} \cong \frac{V_E}{I_C} = \frac{4\text{ V}}{10\text{ mA}} = 400\ \Omega \tag{2–31}$$

Use Thevenin's equivalent circuit to calculate R_1 and R_2 as shown in Figure 2–16.

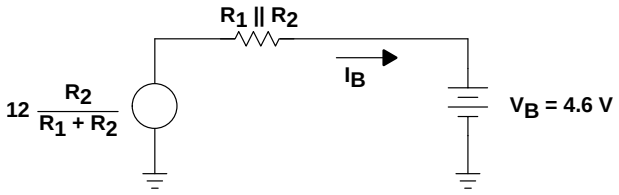


Figure 2–16. Thevenin Equivalent of the Base Circuit

$$I_B = \frac{I_C}{\beta} = \frac{10\text{ mA}}{100} = 0.1\text{ mA} \tag{2–32}$$

$$V_{TH} = \frac{12R_2}{R_1 + R_2} \tag{2–33}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \tag{2–34}$$

We want the base voltage to be 4.6 V because the emitter voltage is then 4 V. Assume a voltage drop of 0.4 V across R_{TH}, so Equation 2–35 can be written. The drop across R_{TH} may not be exactly 0.4 V because of beta variations, but a few hundred mV does not matter is this design. Now, calculate the ratio of R_1 and R_2 using the voltage divider rule (the load current has been accounted for).

$$R_{TH} = \frac{0.4}{0.1}\text{k} = 4\text{ k} \tag{2–35}$$

$$V_{TH} = I_B R_{Th} + V_B = 0.4 + 4.6 = 5 = 12\frac{R_2}{R_1 + R_2} \tag{2–36}$$

$$R_2 = \frac{7}{5} R_1 \tag{2–37}$$

R_1 is almost equal to R_2, thus selecting R_1 as twice the Thevenin resistance yields approximately 4 K as shown in Equation 2–35. Hence, R_1 = 11.2 k and R_2 = 8 k. The ac gain is

approximately R_C/R_{E1} because C_E shorts out R_{E2} at high frequencies, so we can write Equation 2–38.

$$R_{E1} = \frac{R_C}{G} = \frac{400}{4} = 100\ \Omega \tag{2–38}$$

$$R_{E2} = R_E - R_{E1} = 400 - 100 = 300\ \Omega \tag{2–39}$$

The capacitor selection depends on the frequency response required for the amplifier, but 10 μF for C_{IN} and 1000 μF for C_E suffice for a starting point.

Chapter 3

Development of the Ideal Op Amp Equations

Ron Mancini

3.1 Ideal Op Amp Assumptions

The name *Ideal Op Amp* is applied to this and similar analysis because the salient parameters of the op amp are assumed to be perfect. There is no such thing as an ideal op amp, but present day op amps come so close to ideal that *Ideal Op Amp* analysis approaches actual analysis. Op amps depart from the ideal in two ways. First, dc parameters such as input offset voltage are large enough to cause departure from the ideal. The ideal assumes that input offset voltage is zero. Second, ac parameters such as gain are a function of frequency, so they go from large values at dc to small values at high frequencies.

This assumption simplifies the analysis, thus it clears the path for insight. It is so much easier to see the forest when the brush and huge trees are cleared away. Although the ideal op amp analysis makes use of perfect parameters, the analysis is often valid because some op amps approach perfection. In addition, when working at low frequencies, several kHz, the ideal op amp analysis produces accurate answers. Voltage feedback op amps are covered in this chapter, and current feedback op amps are covered in Chapter 8.

Several assumptions have to be made before the ideal op amp analysis can proceed. First, assume that the current flow into the input leads of the op amp is zero. This assumption is almost true in FET op amps where input currents can be less than a pA, but this is not always true in bipolar high-speed op amps where tens of μA input currents are found.

Second, the op amp gain is assumed to be infinite, hence it drives the output voltage to any value to satisfy the input conditions. This assumes that the op amp output voltage can achieve any value. In reality, saturation occurs when the output voltage comes close to a power supply rail, but reality does not negate the assumption, it only bounds it.

Also, implicit in the infinite gain assumption is the need for zero input signal. The gain drives the output voltage until the voltage between the input leads (the error voltage) is zero. This leads to the third assumption that the voltage between the input leads is zero. The implication of zero voltage between the input leads means that if one input is tied to

a hard voltage source such as ground, then the other input is at the same potential. The current flow into the input leads is zero, so the input impedance of the op amp is infinite.

Fourth, the output impedance of the ideal op amp is zero. The ideal op amp can drive any load without an output impedance dropping voltage across it. The output impedance of most op amps is a fraction of an ohm for low current flows, so this assumption is valid in most cases. Fifth, the frequency response of the ideal op amp is flat; this means that the gain does not vary as frequency increases. By constraining the use of the op amp to the low frequencies, we make the frequency response assumption true.

Table 3–1 lists the basic ideal op amp assumptions and FIgure 3–1shows the ideal op amp.

Table 3–1. Basic Ideal Op Amp Assumptions

PARAMETER NAME	PARAMETERS SYMBOL	VALUE
Input current	I_{IN}	0
Input offset voltage	V_{OS}	0
Input impedance	Z_{IN}	∞
Output impedance	Z_{OUT}	0
Gain	a	∞

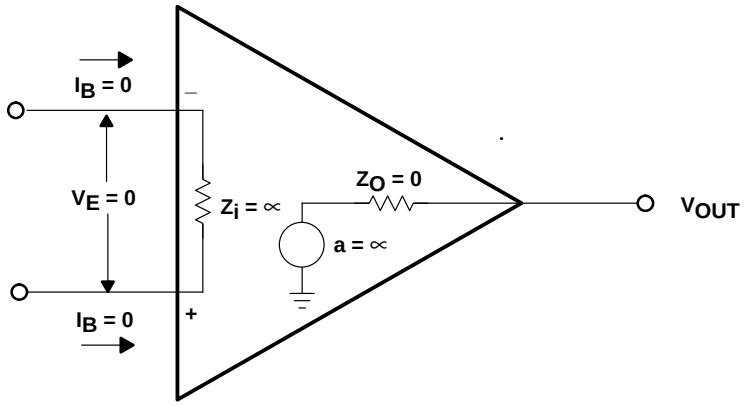


Figure 3–1. The Ideal Op Amp

3.2 The Noninverting Op Amp

The noninverting op amp has the input signal connected to its noninverting input (Figure 3–2), thus its input source sees an infinite impedance. There is no input offset voltage because $V_{OS} = V_E = 0$, hence the negative input must be at the same voltage as the positive input. The op amp output drives current into R_F until the negative input is at the voltage, V_{IN}. This action causes V_{IN} to appear across R_G.

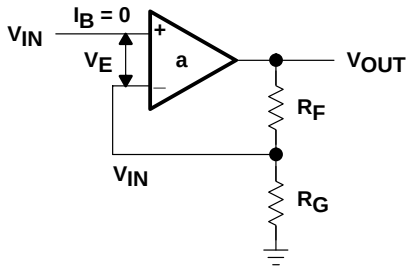


Figure 3–2. The Noninverting Op Amp

The voltage divider rule is used to calculate V_{IN}; V_{OUT} is the input to the voltage divider, and V_{IN} is the output of the voltage divider. Since no current can flow into either op amp lead, use of the voltage divider rule is allowed. Equation 3–1 is written with the aid of the voltage divider rule, and algebraic manipulation yields Equation 3–2 in the form of a gain parameter.

$$V_{IN} = V_{OUT} \frac{R_G}{R_G + R_F} \tag{3–1}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_G + R_F}{R_G} = 1 + \frac{R_F}{R_G} \tag{3–2}$$

When R_G becomes very large with respect to R_F, $(R_F/R_G) \Rightarrow 0$ and Equation 3–2 reduces to Equation 3–3.

$$V_{OUT} = 1 \tag{3–3}$$

Under these conditions $V_{OUT} = 1$ and the circuit becomes a unity gain buffer. R_G is usually deleted to achieve the same results, and when R_G is deleted, R_F can also be deleted (RF must be shorted when it is deleted). When R_F and R_G are deleted, the op amp output is connected to its inverting input with a wire. Some op amps are self-destructive when R_F is left out of the circuit, so R_F is used in many buffer designs. When R_F is included in a buffer circuit, its function is to protect the inverting input from an over voltage to limit the current through the input ESD (electro-static discharge) structure (typically < 1 mA), and it can have almost any value (20 k is often used). R_F can never be left out of the circuit

in a current feedback amplifier design because R_F determines stability in current feedback amplifiers.

Notice that the gain is only a function of the feedback and gain resistors; therefore the feedback has accomplished its function of making the gain independent of the op amp parameters. The gain is adjusted by varying the ratio of the resistors. The actual resistor values are determined by the impedance levels that the designer wants to establish. If R_F = 10 k and R_G = 10 k the gain is two as shown in Equation 2, and if R_F = 100 k and R_G = 100 k the gain is still two. The impedance levels of 10 k or 100 k determine the current drain, the effect of stray capacitance, and a few other points. The impedance level does not set the gain; the ratio of R_F/R_G does.

3.3 The Inverting Op Amp

The noninverting input of the inverting op amp circuit is grounded. One assumption made is that the input error voltage is zero, so the feedback keeps inverting the input of the op amp at a virtual ground (not actual ground but acting like ground). The current flow in the input leads is assumed to be zero, hence the current flowing through R_G equals the current flowing through R_F. Using Kirchoff's law, we write Equation 3–4; and the minus sign is inserted because this is the inverting input. Algebraic manipulation gives Equation 3–5.

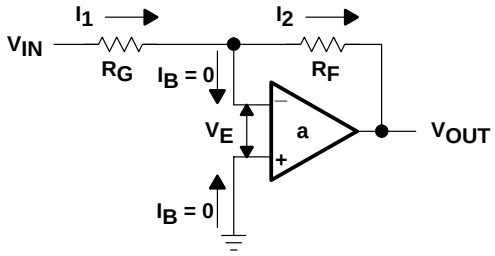


Figure 3–3. The Inverting Op Amp

$$I_1 = \frac{V_{IN}}{R_G} = -I_2 = -\frac{V_{OUT}}{R_F} \tag{3–4}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_G} \tag{3–5}$$

Notice that the gain is only a function of the feedback and gain resistors, so the feedback has accomplished its function of making the gain independent of the op amp parameters. The actual resistor values are determined by the impedance levels that the designer wants to establish. If R_F = 10 k and R_G = 10 k the gain is minus one as shown in Equation

3–5, and if R_F = 100 k and R_G = 100 k the gain is still minus one. The impedance levels of 10 k or 100 k determine the current drain, the effect of stray capacitance, and a few other points. The impedance level does not set the gain; the ratio of R_F/R_G does.

One final note; the output signal is the input signal amplified and inverted. The circuit input impedance is set by R_G because the inverting input is held at a virtual ground.

3.4 The Adder

An adder circuit can be made by connecting more inputs to the inverting op amp (Figure 3–4). The opposite end of the resistor connected to the inverting input is held at virtual ground by the feedback; therefore, adding new inputs does not affect the response of the existing inputs.

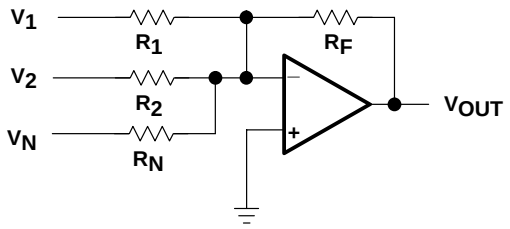


Figure 3–4. The Adder Circuit

Superposition is used to calculate the output voltages resulting from each input, and the output voltages are added algebraically to obtain the total output voltage. Equation 3–6 is the output equation when V_1 and V_2 are grounded. Equations 3–7 and 3–8 are the other superposition equations, and the final result is given in Equation 3–9.

$$V_{OUTN} = -\frac{R_F}{R_N} V_N \tag{3–6}$$

$$V_{OUT1} = -\frac{R_F}{R_1} V_1 \tag{3–7}$$

$$V_{OUT2} = -\frac{R_F}{R_2} V_2 \tag{3–8}$$

$$V_{OUT} = -\left(\frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_N} V_N\right) \tag{3–9}$$

3.5 The Differential Amplifier

The differential amplifier circuit amplifies the difference between signals applied to the inputs (Figure 3–5). Superposition is used to calculate the output voltage resulting from each input voltage, and then the two output voltages are added to arrive at the final output voltage.

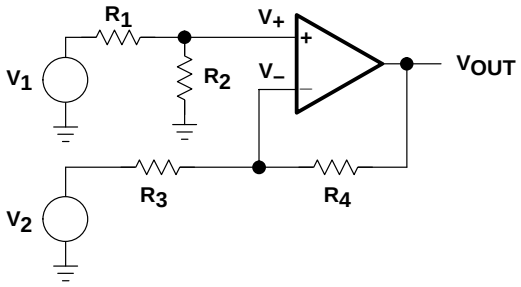


Figure 3–5. The Differential Amplifier

The op amp input voltage resulting from the input source, V_1, is calculated in Equations 3–10 and 3–11. The voltage divider rule is used to calculate the voltage, V_+, and the noninverting gain equation (Equation 3–2) is used to calculate the noninverting output voltage, V_{OUT1}.

$$V_+ = V_1 \frac{R_2}{R_1 + R_2} \tag{3–10}$$

$$V_{OUT1} = V_+(G_+) = V_1 \frac{R_2}{R_1 + R_2}\left(\frac{R_3 + R_4}{R_3}\right) \tag{3–11}$$

The inverting gain equation (Equation 3–5) is used to calculate the stage gain for V_{OUT2} in Equation 3–12. These inverting and noninverting gains are added in Equation 3–13.

$$V_{OUT2} = V_2\left(-\frac{R_4}{R_3}\right) \tag{3–12}$$

$$V_{OUT} = V_1 \frac{R_2}{R_1 + R_2}\left(\frac{R_3 + R_4}{R_3}\right) - V_2 \frac{R_4}{R_3} \tag{3–13}$$

When $R_2 = R_4$ and $R_1 = R_3$, Equation 3–13 reduces to Equation 3–14.

$$V_{OUT} = (V_1 - V_2)\frac{R_4}{R_3} \tag{3–14}$$

It is now obvious that the differential signal, $(V_1–V_2)$, is multiplied by the stage gain, so the name differential amplifier suits the circuit. Because it only amplifies the differential

portion of the input signal, it rejects the common-mode portion of the input signal. A common-mode signal is illustrated in Figure 3–6. Because the differential amplifier strips off or rejects the common-mode signal, this circuit configuration is often employed to strip dc or injected common-mode noise off a signal.

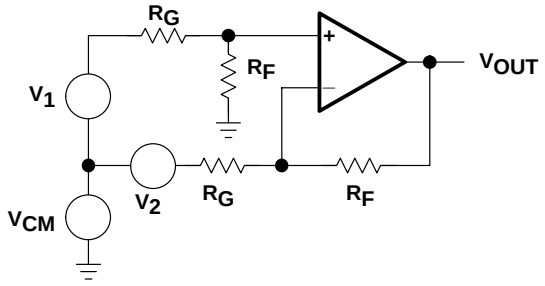


Figure 3–6. Differential Amplifier With Common-Mode Input Signal

The disadvantage of this circuit is that the two input impedances cannot be matched when it functions as a differential amplifier, thus there are two and three op amp versions of this circuit specially designed for high performance applications requiring matched input impedances.

3.6 Complex Feedback Networks

When complex networks are put into the feedback loop, the circuits get harder to analyze because the simple gain equations cannot be used. The usual technique is to write and solve node or loop equations. There is only one input voltage, so superposition is not of any use, but Thevenin's theorem can be used as is shown in the example problem given below.

Sometimes it is desirable to have a low resistance path to ground in the feedback loop. Standard inverting op amps can not do this when the driving circuit sets the input resistor value, and the gain specification sets the feedback resistor value. Inserting a *T* network in the feedback loop (FIgure 3–7) yields a degree of freedom that enables both specifications to be met with a low dc resistance path in the feedback loop.

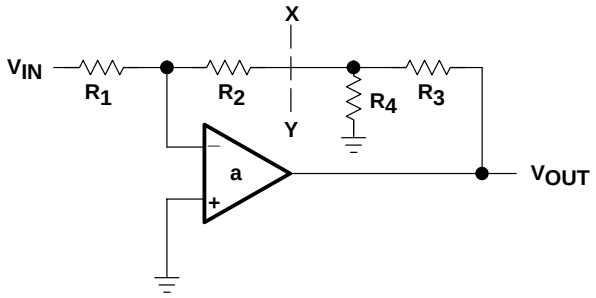


Figure 3–7. T Network in Feedback Loop

Break the circuit at point X–Y, stand on the terminals looking into R_4, and calculate the Thevenin equivalent voltage as shown in Equation 3–15. The Thevenin equivalent impedance is calculated in Equation 3–16.

$$V_{TH} = V_{OUT} \frac{R_4}{R_3 + R_4} \tag{3–15}$$

$$R_{TH} = R_3 \parallel R_4 \tag{3–16}$$

Replace the output circuit with the Thevenin equivalent circuit as shown in Figure 5–8, and calculate the gain with the aid of the inverting gain equation as shown in Equation 3–17.

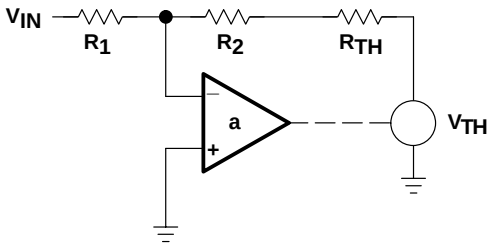


Figure 3–8. Thevenin's Theorem Applied to T Network

Substituting the Thevenin equivalents into Equation 3–17 yields Equation 3–18.

$$-\frac{V_{TH}}{V_{IN}} = \frac{R_2 + R_{TH}}{R_1} \tag{3–17}$$

$$-\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_{TH}}{R_1}\left(\frac{R_3 + R_4}{R_4}\right) = \frac{R_2 + \left(R_3 \parallel R_4\right)}{R_1}\left(\frac{R_3 + R_4}{R_4}\right) \tag{3–18}$$

Algebraic manipulation yields Equation 3–19.

$$-\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_3 + \frac{R_2 R_3}{R_4}}{R_1} \tag{3–19}$$

Specifications for the circuit you are required to build are an inverting amplifier with an input resistance of 10 k (R_G = 10 k), a gain of 100, and a feedback resistance of 20 K or less. The inverting op amp circuit can not meet these specifications because R_F must equal 1000 k. Inserting a *T* network with $R_2 = R_4$ = 10 k and R_3 = 485 k approximately meets the specifications.

3.7 Video Amplifiers

Video signals contain high frequencies, and they use coaxial cable to transmit and receive signals. The cable connecting these circuits has a characteristic impedance of 75 Ω. To prevent reflections, which cause distortion and ghosting, the input and output circuit impedances must match the 75 Ω cable.

Matching the input impedance is simple for a noninverting amplifier because its input impedance is very high; just make R_{IN} = 75 Ω. R_F and R_G can be selected as high values, in the hundreds of Ohms range, so that they have minimal affect on the impedance of the input or output circuit. A matching resistor, R_M, is placed in series with the op amp output to raise its output impedance to 75 Ω; a terminating resistor, R_T, is placed at the input of the next stage to match the cable (Figure 3–9).

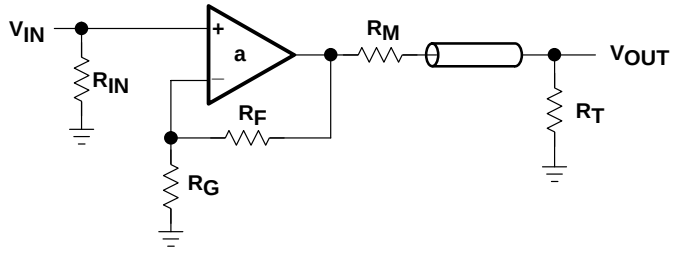


Figure 3–9. Video Amplifier

The matching and terminating resistors are equal in value, and they form a voltage divider of 1/2 because R_T is not loaded. Very often R_F is selected equal to R_G so that the op amp gain equals two. Then the system gain, which is the op amp gain multiplied by the divider gain, is equal to one ($2 \times 1/2 = 1$).

3.8 Capacitors

Capacitors are a key component in a circuit designer's tool kit, thus a short discussion on evaluating their affect on circuit performance is in order. Capacitors have an impedance of $X_C = 1 / 2\pi fC$. Note that when the frequency is zero the capacitive impedance (also known as reactance) is infinite, and that when the frequency is infinite the capacitive impedance is zero. These end-points are derived from the final value theorem, and they are used to get a rough idea of the effect of a capacitor. When a capacitor is used with a resistor, they form what is called a break-point. Without going into complicated math, just accept that the break frequency occurs at $f = 1/(2\pi RC)$ and the gain is –3 dB at the break frequency.

The low pass filter circuit shown in Figure 3–10 has a capacitor in parallel with the feedback resistor. The gain for the low pass filter is given in Equation 3–20.

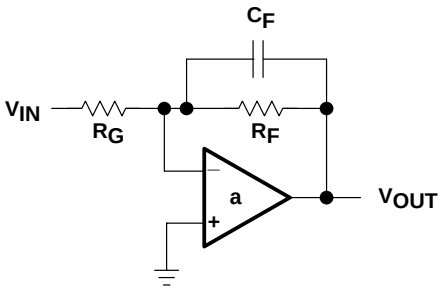


Figure 3–10. Low-Pass Filter

$$\frac{V_{OUT}}{V_{IN}} = -\frac{X_C \parallel R_F}{R_G} \tag{3–20}$$

At very low frequencies $X_C \Rightarrow \infty$, so R_F dominates the parallel combination in Equation 20, and the capacitor has no effect. The gain at low frequencies is $-R_F/R_G$. At very high frequencies $X_C \Rightarrow 0$, so the feedback resistor is shorted out, thus reducing the circuit gain to zero. At the frequency where $X_C = R_F$ the gain is reduced by $\sqrt{2}$ because complex impedances in parallel equal half the vector sum of both impedances.

Connecting the capacitor in parallel with R_G where it has the opposite effect makes a high pass filter (Figure 3–11). Equation 3–21 gives the equation for the high pass filter.

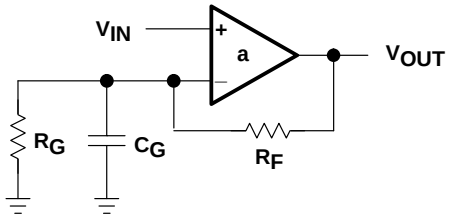


Figure 3–11. High-Pass Filter

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{X_C \parallel R_G} \tag{3–21}$$

At very low frequencies $X_C \Rightarrow \infty$, so R_G dominates the parallel combination in Equation 3–21, and the capacitor has no effect. The gain at low frequencies is $1+R_F/R_G$. At very high frequencies $X_C \Rightarrow 0$, so the gain setting resistor is shorted out thus increasing the circuit gain to maximum.

This simple technique is used to predict the form of a circuit transfer function rapidly. Better analysis techniques are presented in later chapters for those applications requiring more precision.

3.9 Summary

When the proper assumptions are made, the analysis of op amp circuits is straightforward. These assumptions, which include zero input current, zero input offset voltage, and infinite gain, are realistic assumptions because the new op amps make them true in most applications.

When the signal is comprised of low frequencies, the gain assumption is valid because op amps have very high gain at low frequencies. When CMOS op amps are used, the input current is in the femto amp range; close enough to zero for most applications. Laser trimmed input circuits reduce the input offset voltage to a few micro volts; close enough to zero for most applications. The ideal op amp is becoming real; especially for undemanding applications.

Chapter 4

Single-Supply Op Amp Design Techniques

Ron Mancini

4.1 Single Supply versus Dual Supply

The previous chapter assumed that all op amps were powered from dual or split supplies, and this is not the case in today's world of portable, battery-powered equipment. When op amps are powered from dual supplies (see Figure 4–1), the supplies are normally equal in magnitude, opposing in polarity, and the center tap of the supplies is connected to ground. Any input sources connected to ground are automatically referenced to the center of the supply voltage, so the output voltage is automatically referenced to ground.

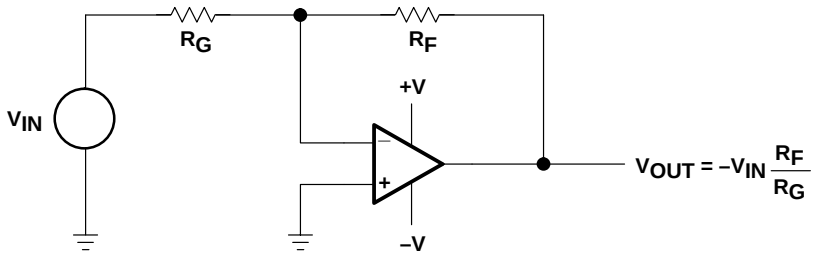


Figure 4–1. Split-Supply Op Amp Circuit

Single-supply systems do not have the convenient ground reference that dual-supply systems have, thus biasing must be employed to ensure that the output voltage swings between the correct voltages. Input sources connected to ground are actually connected to a supply rail in single-supply systems. This is analogous to connecting a dual-supply input to the minus power rail. This requirement for biasing the op amp inputs to achieve the desired output voltage swing complicates single-supply designs.

When the signal source is not referenced to ground (see Figure 4–2), the voltage difference between ground and the reference voltage is amplified along with the signal. Unless the reference voltage was inserted as a bias voltage, and such is not the case when the input signal is connected to ground, the reference voltage must be stripped from the signal so that the op amp can provide maximum dynamic range.

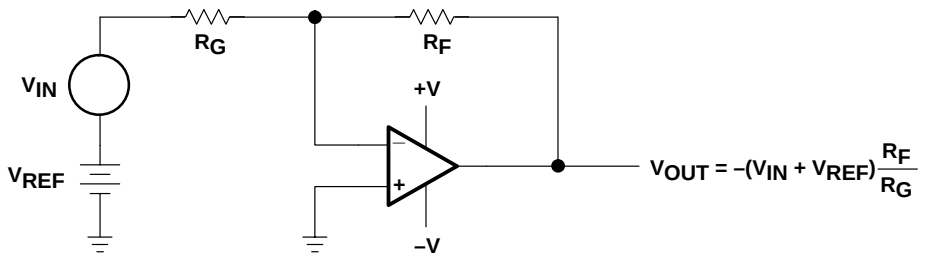


Figure 4–2. Split-Supply Op Amp Circuit With Reference Voltage Input

An input bias voltage is used to eliminate the reference voltage when it must not appear in the output voltage (see Figure 4–3). The voltage, V_{REF}, is in both input circuits, hence it is named a common-mode voltage. Voltage feedback op amps reject common-mode voltages because their input circuit is constructed with a differential amplifier (chosen because it has natural common-mode voltage rejection capabilities).

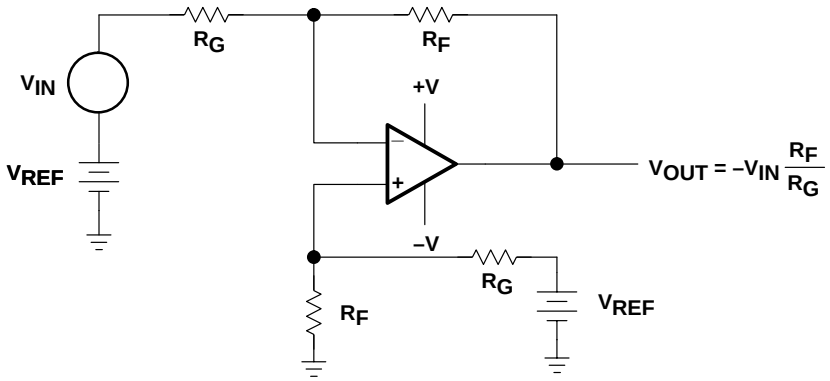


Figure 4–3. Split-Supply Op Amp Circuit With Common-Mode Voltage

When signal sources are referenced to ground, single-supply op amp circuits exhibit a large input common-mode voltage. Figure 4–4 shows a single-supply op amp circuit that has its input voltage referenced to ground. The input voltage is not referenced to the midpoint of the supplies like it would be in a split-supply application, rather it is referenced to the lower power supply rail. This circuit does not operate when the input voltage is positive because the output voltage would have to go to a negative voltage, hard to do with a positive supply. It operates marginally with small negative input voltages because most op amps do not function well when the inputs are connected to the supply rails.

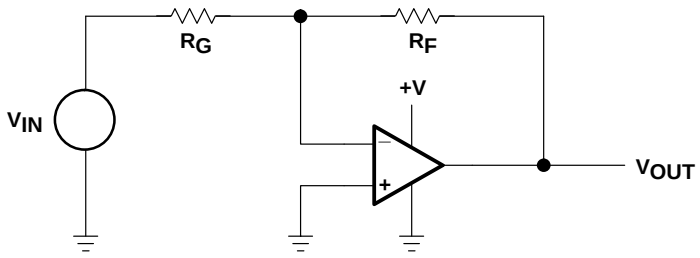


Figure 4–4. Single-Supply Op Amp Circuit

The constant requirement to account for inputs connected to ground or different reference voltages makes it difficult to design single-supply op amp circuits. Unless otherwise specified, all op amp circuits discussed in this chapter are single-supply circuits. The single-supply may be wired with the negative or positive lead connected to ground, but as long as the supply polarity is correct, the wiring does not affect circuit operation.

Use of a single-supply limits the polarity of the output voltage. When the supply voltage $V_{CC} = 10$ V, the output voltage is limited to the range $0 \leq V_{out} \leq 10$. This limitation precludes negative output voltages when the circuit has a positive supply voltage, but it does not preclude negative input voltages when the circuit has a positive supply voltage. As long as the voltage on the op amp input leads does not become negative, the circuit can handle negative input voltages.

Beware of working with negative (positive) input voltages when the op amp is powered from a positive (negative) supply because op amp inputs are highly susceptible to reverse voltage breakdown. Also, insure that all possible start-up conditions do not reverse bias the op amp inputs when the input and supply voltage are opposite polarity.

4.2 Circuit Analysis

The complexities of single-supply op amp design are illustrated with the following example. Notice that the biasing requirement complicates the analysis by presenting several conditions that are not realizable. It is best to wade through this material to gain an understanding of the problem, especially since a cookbook solution is given later in this chapter. The previous chapter assumed that the op amps were ideal, and this chapter starts to deal with op amp deficiencies. The input and output voltage swing of many op amps are limited as shown in Figure 4–7, but if one designs with the selected rail-to-rail op amps, the input/output swing problems are minimized. The inverting circuit shown in Figure 4–5 is analyzed first.

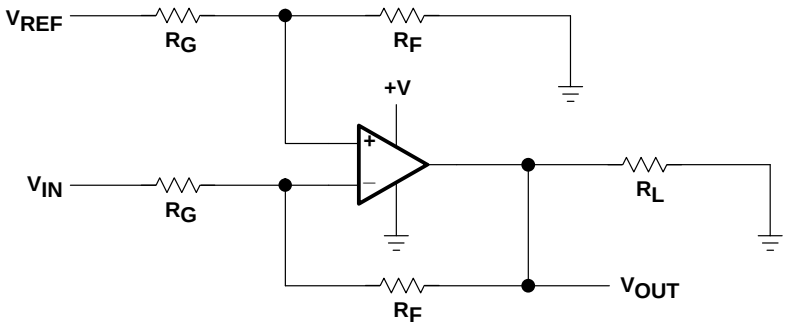


Figure 4–5. Inverting Op Amp

Equation 4–1 is written with the aid of superposition, and simplified algebraically, to acquire Equation 4–2.

$$V_{OUT} = V_{REF}\left(\frac{R_F}{R_G + R_F}\right)\left(\frac{R_F + R_G}{R_G}\right) - V_{IN}\frac{R_F}{R_G} \tag{4–1}$$

$$V_{OUT} = \left(V_{REF} - V_{IN}\right)\frac{R_F}{R_G} \tag{4–2}$$

As long as the load resistor, R_L, is a large value, it does not enter into the circuit calculations, but it can introduce some second order effects such as limiting the output voltage swings. Equation 4–3 is obtained by setting V_{REF} equal to V_{IN}, and there is no output voltage from the circuit regardless of the input voltage. The author unintentionally designed a few of these circuits before he created an orderly method of op amp circuit design. Actually, a real circuit has a small output voltage equal to the lower transistor saturation voltage, which is about 150 mV for a TLC07X.

$$V_{OUT} = \left(V_{REF} - V_{IN}\right)\frac{R_F}{R_G} = \left(V_{IN} - V_{IN}\right)\frac{R_F}{R_G} = 0 \tag{4–3}$$

When $V_{REF} = 0$, $V_{OUT} = -V_{IN}(R_F/R_G)$, there are two possible solutions to Equation 4–2. First, when V_{IN} is any positive voltage, V_{OUT} should be negative voltage. The circuit can not achieve a negative voltage with a positive supply, so the output saturates at the lower power supply rail. Second, when V_{IN} is any negative voltage, the output spans the normal range according to Equation 4–5.

$$V_{IN} \geq 0, \qquad V_{OUT} = 0 \tag{4–4}$$

$$V_{IN} \leq 0, \qquad V_{OUT} = \left|V_{IN}\right| \frac{R_F}{R_G} \tag{4–5}$$

When V_{REF} equals the supply voltage, V_{CC}, we obtain Equation 4–6. In Equation 4–6, when V_{IN} is negative, V_{OUT} should exceed V_{CC}; that is impossible, so the output saturates. When V_{IN} is positive, the circuit acts as an inverting amplifier.

$$V_{OUT} = \left(V_{CC} - V_{IN}\right)\frac{R_F}{R_G} \quad (4\text{–}6)$$

The transfer curve for the circuit shown in Figure 4–6 (V_{CC} = 5 V, $R_G = R_F$ = 100 kΩ, R_L = 10 kΩ) is shown in Figure 4–7.

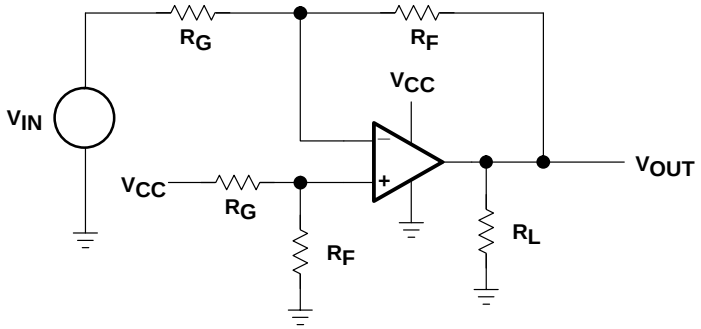


Figure 4–6. Inverting Op Amp With V_{CC} Bias

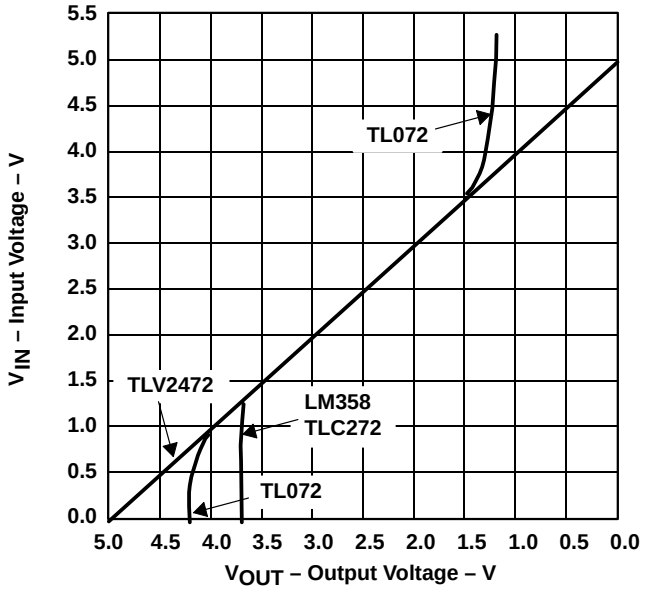


Figure 4–7. Transfer Curve for Inverting Op Amp With V_{CC} Bias

Four op amps were tested in the circuit configuration shown in Figure 4–6. Three of the old generation op amps, LM358, TL07X, and TLC272 had output voltage spans of 2.3 V to 3.75 V. This performance does not justify the ideal op amp assumption that was made in the previous chapter unless the output voltage swing is severely limited. Limited output or input voltage swing is one of the worst deficiencies a single-supply op amp can have because the limited voltage swing limits the circuit's dynamic range. Also, limited voltage swing frequently results in distortion of large signals. The fourth op amp tested was the newer TLV247X, which was designed for rail-to-rail operation in single-supply circuits. The TLV247X plotted a perfect curve (results limited by the instrumentation), and it amazed the author with a textbook performance that justifies the use of ideal assumptions. Some of the older op amps must limit their transfer equation as shown in Equation 4–7.

$$V_{OUT} = \left(V_{CC} - V_{IN}\right)\frac{R_F}{R_G} \quad \text{for} \quad V_{OH} \geq V_{OUT} \geq V_{OL} \tag{4–7}$$

The noninverting op amp circuit is shown in Figure 4–8. Equation 4–8 is written with the aid of superposition, and simplified algebraically, to acquire Equation 4–9.

$$V_{OUT} = V_{IN}\left(\frac{R_F}{R_G + R_F}\right)\left(\frac{R_F + R_G}{R_G}\right) - V_{REF}\,\frac{R_F}{R_G} \tag{4–8}$$

$$V_{OUT} = \left(V_{IN} - V_{REF}\right)\frac{R_F}{R_G} \tag{4–9}$$

When $V_{REF} = 0$, $V_{OUT} = V_{IN}\,\frac{R_F}{R_G}$, there are two possible circuit solutions. First, when V_{IN} is a negative voltage, V_{OUT} must be a negative voltage. The circuit can not achieve a negative output voltage with a positive supply, so the output saturates at the lower power supply rail. Second, when V_{IN} is a positive voltage, the output spans the normal range as shown by Equation 4–11.

$$V_{IN} \leq 0, \qquad V_{OUT} = 0 \tag{4–10}$$

$$V_{IN} \geq 0, \qquad V_{OUT} = V_{IN} \tag{4–11}$$

The noninverting op amp circuit is shown in Figure 4–8 with $V_{CC} = 5$ V, $R_G = R_F = 100$ kΩ, and $R_L = 10$ kΩ. The transfer curve for this circuit is shown in Figure 4–9; a TLV247X serves as the op amp.

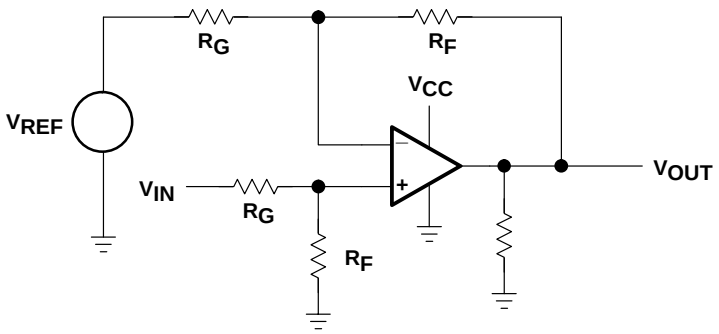


Figure 4–8. Noninverting Op Amp

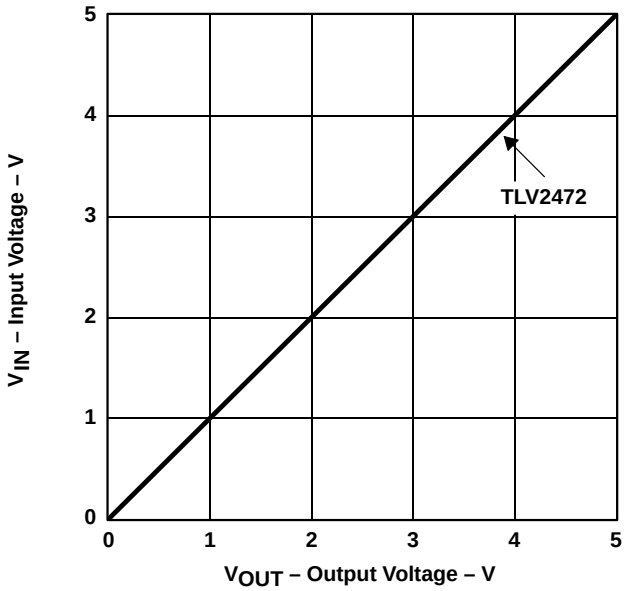


Figure 4–9. Transfer Curve for Noninverting Op Amp

There are many possible variations of inverting and noninverting circuits. At this point many designers analyze these variations hoping to stumble upon the one that solves the circuit problem. Rather than analyze each circuit, it is better to learn how to employ simultaneous equations to render specified data into equation form. When the form of the desired equation is known, a circuit that fits the equation is chosen to solve the problem. The resulting equation must be a straight line, thus there are only four possible solutions.

4.3 Simultaneous Equations

Taking an orderly path to developing a circuit that works the first time starts here; follow these steps until the equation of the op amp is determined. Use the specifications given for the circuit coupled with simultaneous equations to determine what form the op amp equation must have. Go to the section that illustrates that equation form (called a case), solve the equation to determine the resistor values, and you have a working solution.

A linear op amp transfer function is limited to the equation of a straight line (Equation 4–12).

$$y = \pm\ mx \pm b \tag{4–12}$$

The equation of a straight line has four possible solutions depending upon the sign of m, the slope, and b, the intercept; thus simultaneous equations yield solutions in four forms. Four circuits must be developed; one for each form of the equation of a straight line. The four equations, cases, or forms of a straight line are given in Equations 4–13 through 4–16, where electronic terminology has been substituted for math terminology.

$$V_{OUT} = +\ mV_{IN} + b \tag{4–13}$$

$$V_{OUT} = +\ mV_{IN} - b \tag{4–14}$$

$$V_{OUT} = -\ mV_{IN} + b \tag{4–15}$$

$$V_{OUT} = -\ mV_{IN} - b \tag{4–16}$$

Given a set of two data points for V_{OUT} and V_{IN}, simultaneous equations are solved to determine m and b for the equation that satisfies the given data. The sign of m and b determines the type of circuit required to implement the solution. The given data is derived from the specifications; i. e., a sensor output signal ranging from 0.1 V to 0.2 V must be interfaced into an analog-to-digital converter that has an input voltage range of 1 V to 4 V. These data points (V_{OUT} = 1 V @ V_{IN} = 0.1 V, V_{OUT} = 4 V @ V_{IN} = 0.2 V) are inserted into Equation 4–13, as shown in Equations 4–17 and 4–18, to obtain m and b for the specifications.

$$1 = m(0.1) + b \tag{4–17}$$

$$4 = m(0.2) + b \tag{4–18}$$

Multiply Equation 4–17 by 2 and subtract it from Equation 4–18.

$$2 = m(0.2) + 2b \tag{4–19}$$

$$b = -2 \tag{4–20}$$

After algebraic manipulation of Equation 4–17, substitute Equation 4–20 into Equation 4–17 to obtain Equation 4–21.

$$m = \frac{2 + 1}{0.1} = 30 \tag{4–21}$$

Now m and b are substituted back into Equation 4–13 yielding Equation 4–22.

$$V_{OUT} = 30V_{IN} - 2 \tag{4–22}$$

Notice, although Equation 4–13 was the starting point, the form of Equation 4–22 is identical to the format of Equation 4–14. The specifications or given data determine the sign of m and b, and starting with Equation 4–13, the final equation form is discovered after m and b are calculated. The next step required to complete the problem solution is to develop a circuit that has an m = 30 and b = –2. Circuits were developed for Equations 4–13 through 4–16, and they are given under the headings Case 1 through Case 4 respectively. There are different circuits that will yield the same equations, but these circuits were selected because they do not require negative references.

4.3.1 Case 1: $V_{OUT} = +mV_{IN}+b$

The circuit configuration that yields a solution for Case 1 is shown in Figure 4–10. The figure includes two 0.01-µF capacitors. These capacitors are called decoupling capacitors, and they are included to reduce noise and provide increased noise immunity. Sometimes two 0.01-µF capacitors serve this purpose, sometimes more extensive filtering is needed, and sometimes one capacitor serves this purpose. Special attention must be paid to the regulation and noise content of V_{CC} when V_{CC} is used as a reference because some portion of the noise content of V_{CC} will be multiplied by the circuit gain.

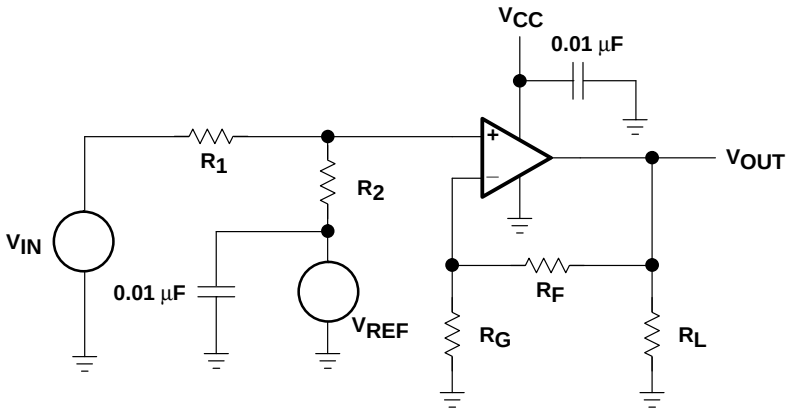


Figure 4–10. Schematic for Case1: $V_{OUT} = +mV_{IN} + b$

The circuit equation is written using the voltage divider rule and superposition.

$$V_{OUT} = V_{IN}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) + V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \quad (4–23)$$

The equation of a straight line (case 1) is repeated in Equation 4–24 below so comparisons can be made between it and Equation 4–23.

$$V_{OUT} = mV_{IN} + b \quad (4–24)$$

Equating coefficients yields Equations 4–25 and 4–26.

$$m = \left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \quad (4–25)$$

$$b = V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \quad (4–26)$$

Example; the circuit specifications are V_{OUT} = 1 V at V_{IN} = 0.01 V, V_{OUT} = 4.5 V at V_{IN} = 1 V, R_L = 10 k, five percent resistor tolerances, and V_{CC} = 5 V. No reference voltage is available, thus V_{CC} is used for the reference input, and V_{REF} = 5 V. A reference voltage source is left out of the design as a space and cost savings measure, and it sacrifices noise performance, accuracy, and stability performance. Cost is an important specification, but the V_{CC} supply must be specified well enough to do the job. Each step in the subsequent design procedure is included in this analysis to ease learning and increase boredom. Many steps are skipped when subsequent cases are analyzed.

The data is substituted into simultaneous equations.

$$1 = m(0.01) + b \quad (4–27)$$

$$4.5 = m(1.0) + b \quad (4–28)$$

Equation 4–27 is multiplied by 100 (Equation 4–29) and Equation 4–28 is subtracted from Equation 4–29 to obtain Equation 4–30.

$$100 = m(1.0) + 100b \quad (4–29)$$

$$b = \frac{95.5}{99} = 0.9646 \quad (4–30)$$

The slope of the transfer function, m, is obtained by substituting b into Equation 4–27.

$$m = \frac{1–b}{0.01} = \frac{1–0.9646}{0.01} = 3.535 \quad (4–31)$$

Now that b and m are calculated, the resistor values can be calculated. Equations 4–25 and 4–26 are solved for the quantity $(R_F + R_G)/R_G$, and then they are set equal in Equation 4–32 thus yielding Equation 4–33.

$$\frac{R_F + R_G}{R_G} = m\left(\frac{R_1 + R_2}{R_2}\right) = \frac{b}{V_{CC}}\left(\frac{R_1 + R_2}{R_1}\right) \tag{4–32}$$

$$R_2 = \frac{3.535}{\frac{0.9646}{5}} R_1 = 18.316 R_1 \tag{4–33}$$

Five percent tolerance resistors are specified for this design, so we choose R_1 = 10 kΩ, and that sets the value of R_2 = 183.16 kΩ. The closest 5% resistor value to 183.16 kΩ is 180 kΩ; therefore, select R_1 = 10 kΩ and R_2 = 180 kΩ. Being forced to yield to reality by choosing standard resistor values means that there is an error in the circuit transfer function because m and b are not exactly the same as calculated. The real world constantly forces compromises into circuit design, but the good circuit designer accepts the challenge and throws money or brains at the challenge. Resistor values closer to the calculated values could be selected by using 1% or 0.5% resistors, but that selection increases cost and violates the design specification. The cost increase is hard to justify except in precision circuits. Using ten-cent resistors with a ten-cent op amp usually is false economy.

The left half of Equation 4–32 is used to calculate R_F and R_G.

$$\frac{R_F + R_G}{R_G} = m\left(\frac{R_1 + R_2}{R_2}\right) = 3.535\left(\frac{180 + 10}{180}\right) = 3.73 \tag{4–34}$$

$$R_F = 2.73 R_G \tag{4–35}$$

The resulting circuit equation is given below.

$$V_{OUT} = 3.5 V_{IN} + 0.97 \tag{4–36}$$

The gain setting resistor, R_G, is selected as 10 kΩ, and 27 kΩ, the closest 5% standard value is selected for the feedback resistor, R_F. Again, there is a slight error involved with standard resistor values. This circuit must have an output voltage swing from 1 V to 4.5 V. The older op amps can not be used in this circuit because they lack dynamic range, so the TLV247X family of op amps is selected. The data shown in Figure 4–7 confirms the op amp selection because there is little error. The circuit with the selected component values is shown in Figure 4–11. The circuit was built with the specified components, and the transfer curve is shown in Figure 4–12.

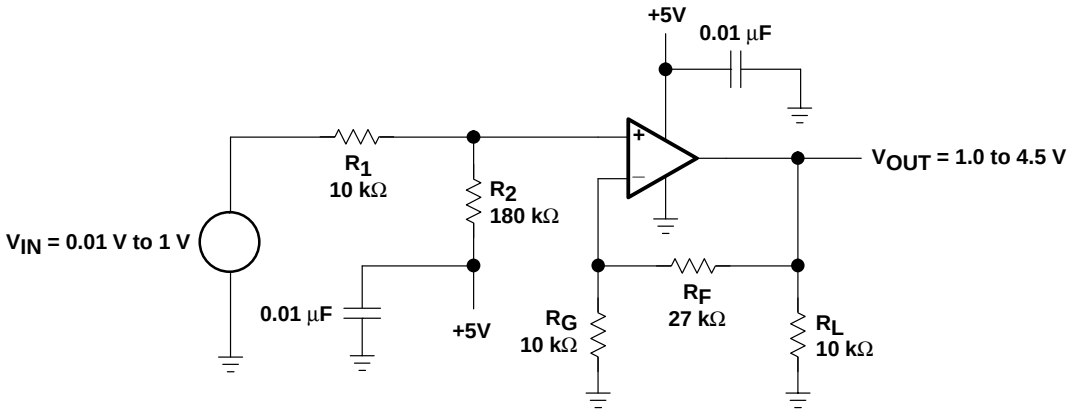


Figure 4–11. Case 1 Example Circuit

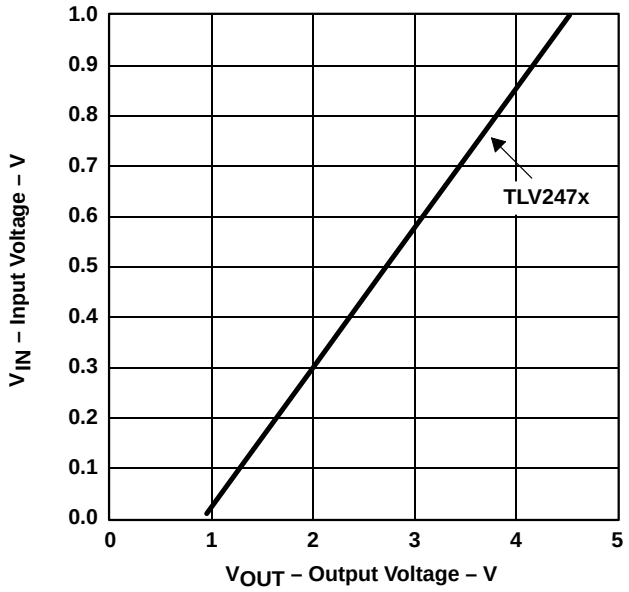


Figure 4–12. Case 1 Example Circuit Measured Transfer Curve

The transfer curve shown is a straight line, and that means that the circuit is linear. The V_{OUT} intercept is about 0.98 V rather than 1 V as specified, and this is excellent performance considering that the components were selected randomly from bins of resistors. Different sets of components would have slightly different slopes because of the resistor tolerances. The TLV247X has input bias currents and input offset voltages, but the effect of these errors is hard to measure on the scale of the output voltage. The output voltage

measured 4.53 V when the input voltage was 1 V. Considering the low and high input voltage errors, it is safe to conclude that the resistor tolerances have skewed the gain slightly, but this is still excellent performance for 5% components. Often lab data similar to that shown here is more accurate than the 5% resistor tolerance, but do not fall into the trap of expecting this performance, because you will be disappointed if you do.

The resistors were selected in the k-Ω range arbitrarily. The gain and offset specifications determine the resistor ratios, but supply current, frequency response, and op amp drive capability determine their absolute values. The resistor value selection in this design is high because modern op amps do not have input current offset problems, and they yield reasonable frequency response. If higher frequency response is demanded, the resistor values must decrease, and resistor value decreases reduce input current errors, while supply current increases. When the resistor values get low enough, it becomes hard for another circuit, or possibly the op amp, to drive the resistors.

4.3.2 Case 2: $V_{OUT} = +mV_{IN} - b$

The circuit shown in Figure 4–13 yields a solution for Case 2. The circuit equation is obtained by taking the Thevenin equivalent circuit looking into the junction of R_1 and R_2. After the R_1, R_2 circuit is replaced with the Thevenin equivalent circuit, the gain is calculated with the ideal gain equation (Equation 4–37).

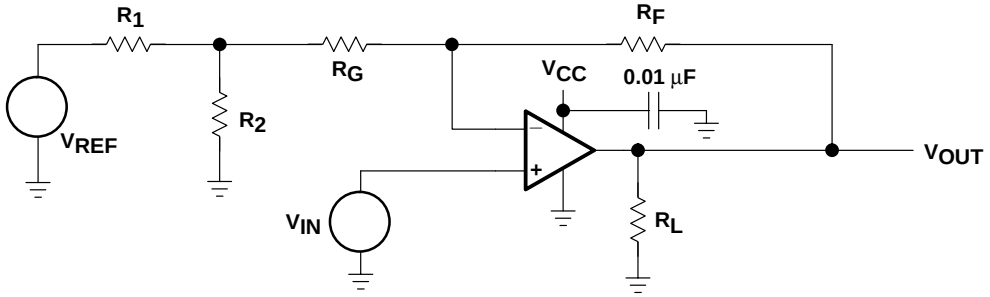


Figure 4–13. Schematic for Case 2: $V_{OUT} = +mV_{IN} - b$

$$V_{OUT} = V_{IN}\left(\frac{R_F + R_G + R_1 \parallel R_2}{R_G + R_1 \parallel R_2}\right) - V_{REF}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1 \parallel R_2}\right) \qquad (4\text{–}37)$$

Comparing terms in Equations 4–37 and 4–14 enables the extraction of m and b.

$$m = \frac{R_F + R_G + R_1 \parallel R_2}{R_G + R_1 \parallel R_2} \tag{4–38}$$

$$|b| = V_{REF}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1 \parallel R_2}\right) \tag{4–39}$$

The specifications for an example design are: V_{OUT} = 1.5 V @ V_{IN} = 0.2 V, V_{OUT} = 4.5 V @ V_{IN} = 0.5 V, $V_{REF} = V_{CC}$ = 5 V, R_L = 10 kΩ, and 5% resistor tolerances. The simultaneous equations, (Equations 4–40 and 4–41), are written below.

$$1.5 = 0.2m + b \tag{4–40}$$

$$4.5 = 0.5m + b \tag{4–41}$$

From these equations we find that b = -0.5 and m = 10. Making the assumption that $R_1||R_2 << R_G$ simplifies the calculations of the resistor values.

$$m = 10 = \frac{R_F + R_G}{R_G} \tag{4–42}$$

$$R_F = 9R_G \tag{4–43}$$

Let R_G = 20 kΩ, and then R_F = 180 kΩ.

$$b = V_{CC}\left(\frac{R_F}{R_G}\right)\left(\frac{R_2}{R_1 + R_2}\right) = 5\left(\frac{180}{20}\right)\left(\frac{R_2}{R_1 + R_2}\right) \tag{4–44}$$

$$R_1 = \frac{1–0.01111}{0.01111}R_2 = 89R_2 \tag{4–45}$$

Select R_2 = 0.82 kΩ and R_1 equals 72.98 kΩ. Since 72.98 kΩ is not a standard 5% resistor value, R_1 is selected as 75 kΩ. The difference between the selected and calculated value of R_1 has about a 3% effect on b, and this error shows up in the transfer function as an intercept rather than a slope error. The parallel resistance of R_1 and R_2 is approximately 0.82 kΩ and this is much less than R_G, which is 20 kΩ, thus the earlier assumption that $R_G >> R1||R2$ is justified. R_2 could have been selected as a smaller value, but the smaller values yielded poor standard 5% values for R_1. The final circuit is shown in Figure 4–14 and the measured transfer curve for this circuit is shown in Figure 4–15.

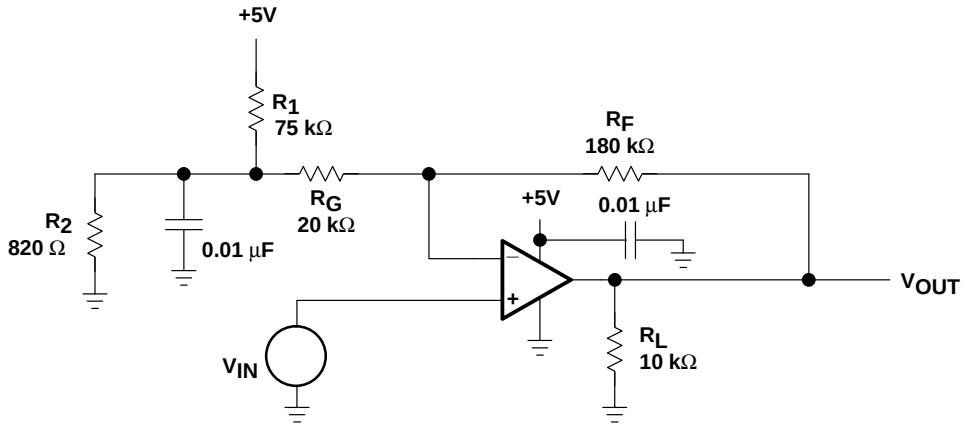


Figure 4–14. Case 2 Example Circuit

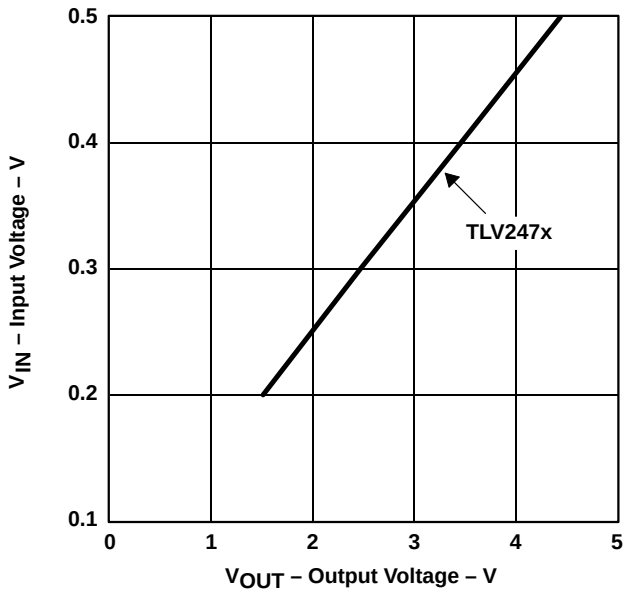


Figure 4–15. Case 2 Example Circuit Measured Transfer Curve

The TLV247X was used to build the test circuit because of its wide dynamic range. The transfer curve plots very close to the theoretical curve; the direct result of using a high performance op amp.

4.3.3 Case 3: $V_{OUT} = -mV_{IN} + b$

The circuit shown in Figure 4–16 yields the transfer function desired for Case 3.

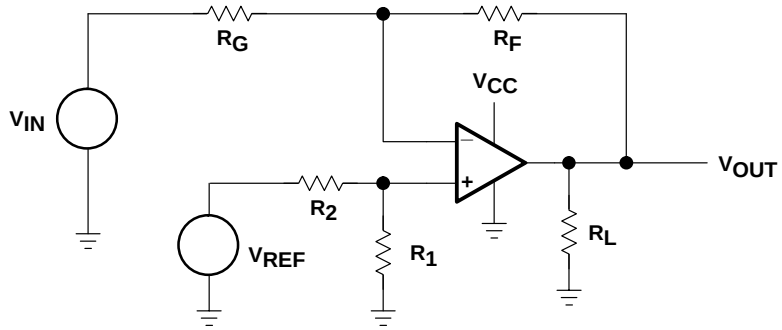


Figure 4–16. Schematic for Case 3: $V_{OUT} = -mV_{IN} + b$

The circuit equation is obtained with superposition.

$$V_{OUT} = -V_{IN}\left(\frac{R_F}{R_G}\right) + V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \quad (4–46)$$

Comparing terms between Equations 4–45 and 4–15 enables the extraction of m and b.

$$|m| = \frac{R_F}{R_G} \quad (4–47)$$

$$b = V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \quad (4–48)$$

The design specifications for an example circuit are: V_{OUT} = 1 V @ V_{IN} = -0.1 V, V_{OUT} = 6 V @ V_{IN} = -1 V, $V_{REF} = V_{CC}$ = 10 V, R_L = 100 Ω, and 5% resistor tolerances. The supply voltage available for this circuit is 10 V, and this exceeds the maximum allowable supply voltage for the TLV247X. Also, this circuit must drive a back-terminated cable that looks like two 50-Ω resistors connected in series, thus the op amp must be able to drive 6/100 = 60 mA. The stringent op amp selection criteria limits the choice to relatively new op amps if ideal op amp equations are going to be used. The TLC07X has excellent single-supply input performance coupled with high output current drive capability, so it is selected for this circuit. The simultaneous equations (Equations 4–49 and 4–50), are written below.

$$1 = (-0.1)m + b \quad (4–49)$$

$$6 = (-1)m + b \quad (4–50)$$

From these equations we find that b = 0.444 and m = –5.6.

$$|m| = 5.56 = \frac{R_F}{R_G} \tag{4–51}$$

$$R_F = 5.56R_G \tag{4–52}$$

Let R_G = 10 kΩ, and then R_F = 56.6 kΩ, which is not a standard 5% value, hence R_F is selected as 56 kΩ.

$$b = V_{CC}\left(\frac{R_F + R_G}{R_G}\right)\left(\frac{R_1}{R_1 + R_2}\right) = 10\left(\frac{56 + 10}{10}\right)\left(\frac{R_1}{R_1 + R_2}\right) \tag{4–53}$$

$$R_2 = \frac{66–0.4444}{0.4444}R_1 = 147.64R_1 \tag{4–54}$$

The final equation for the example is given below

$$V_{OUT} = -5.56V_{IN} + 0.444 \tag{4–55}$$

Select R_1 = 2 kΩ and R_2 = 295.28 kΩ. Since 295.28 kΩ is not a standard 5% resistor value, R_1 is selected as 300 kΩ. The difference between the selected and calculated value of R_1 has a nearly insignificant effect on b. The final circuit is shown in Figure 4–17, and the measured transfer curve for this circuit is shown in Figure 4–18.

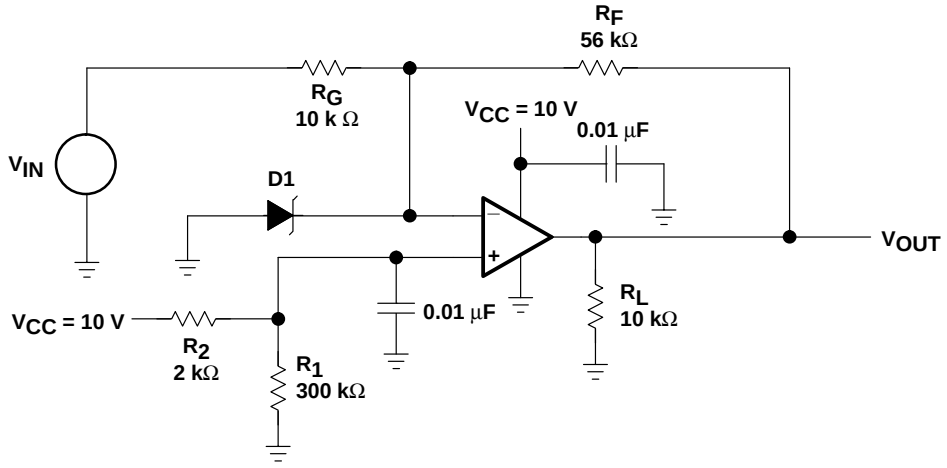


Figure 4–17. Case 3 Example Circuit

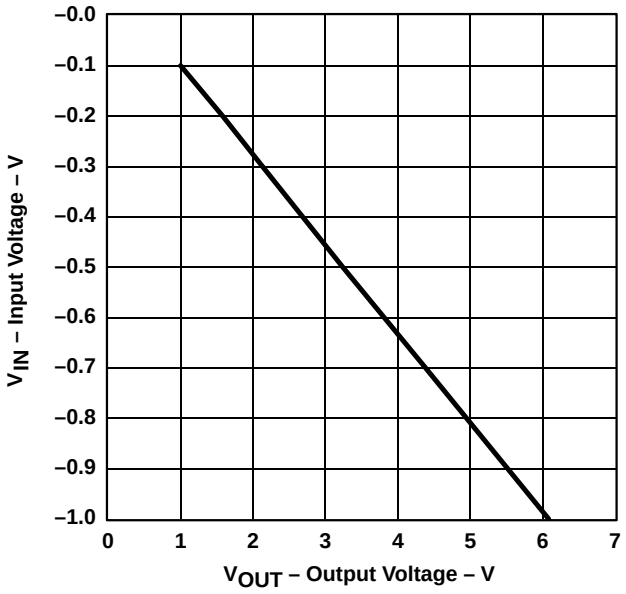


Figure 4–18. Case 3 Example Circuit Measured Transfer Curve

As long as the circuit works normally, there are no problems handling the negative voltage input to the circuit, because the inverting lead of the TLC07X is at a positive voltage. The positive op amp input lead is at a voltage of approximately 65 mV, and normal op amp operation keeps the inverting op amp input lead at the same voltage because of the assumption that the error voltage is zero. When V_{CC} is powered down while there is a negative voltage on the input circuit, most of the negative voltage appears on the inverting op amp input lead.

The most prudent solution is to connect the diode, D_1, with its cathode on the inverting op amp input lead and its anode at ground. If a negative voltage gets on the inverting op amp input lead, it is clamped to ground by the diode. Select the diode type as germanium or Schottky so the voltage drop across the diode is about 200 mV; this small voltage does not harm most op amp inputs. As a further precaution, R_G can be split into two resistors with the diode inserted at the junction of the two resistors. This places a current limiting resistor between the diode and the inverting op amp input lead.

4.3.4 Case 4: $V_{OUT} = -mV_{IN} - b$

The circuit shown in Figure 4–19 yields a solution for Case 4. The circuit equation is obtained by using superposition to calculate the response to each input. The individual responses to V_{IN} and V_{REF} are added to obtain Equation 4–56.

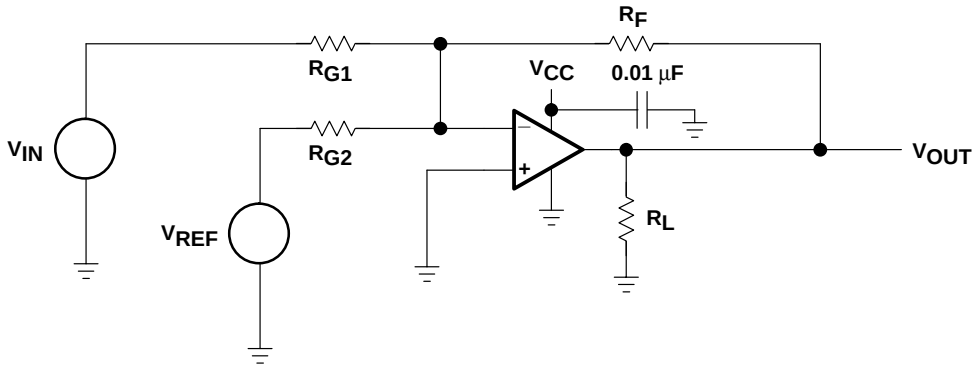


Figure 4–19. Schematic for Case 4: $V_{OUT} = -mV_{IN} - b$

$$V_{OUT} = -V_{IN}\frac{R_F}{R_{G1}} - V_{REF}\frac{R_F}{R_{G2}} \tag{4–56}$$

Comparing terms in Equations 4–56 and 4–16 enables the extraction of m and b.

$$|m| = \frac{R_F}{R_{G1}} \tag{4–57}$$

$$|b| = V_{REF}\frac{R_F}{R_{G2}} \tag{4–58}$$

The design specifications for an example circuit are: V_{OUT} = 1 V @ V_{IN} = –0.1 V, V_{OUT} = 5 V @ V_{IN} =– 0.3 V, $V_{REF} = V_{CC}$ = 5 V, R_L = 10 kΩ, and 5% resistor tolerances. The simultaneous Equations 4–59 and 4–60, are written below.

$$1 = (-0.1)m + b \tag{4–59}$$

$$5 = (-0.3)m + b \tag{4–60}$$

From these equations we find that b = –1 and m = –20. Setting the magnitude of m equal to Equation 4–57 yields Equation 4–61.

$$|m| = 20 = \frac{R_F}{R_{G1}} \tag{4–61}$$

$$R_F = 20R_{G1} \tag{4–62}$$

Let R_{G1} = 1 kΩ, and then R_F = 20 kΩ.

$$|b| = V_{CC}\left(\frac{R_F}{R_{G1}}\right) = 5\left(\frac{R_F}{R_{G2}}\right) = 1 \quad (4–63)$$

$$R_{G2} = \frac{R_F}{0.2} = \frac{20}{0.2} = 100\ k\Omega \quad (4–64)$$

The final equation for this example is given in Equation 4–63.

$$V_{OUT} = -20V_{IN} - 1 \quad (4–65)$$

The final circuit is shown in Figure 4–20 and the measured transfer curve for this circuit is shown in Figure 4–21.

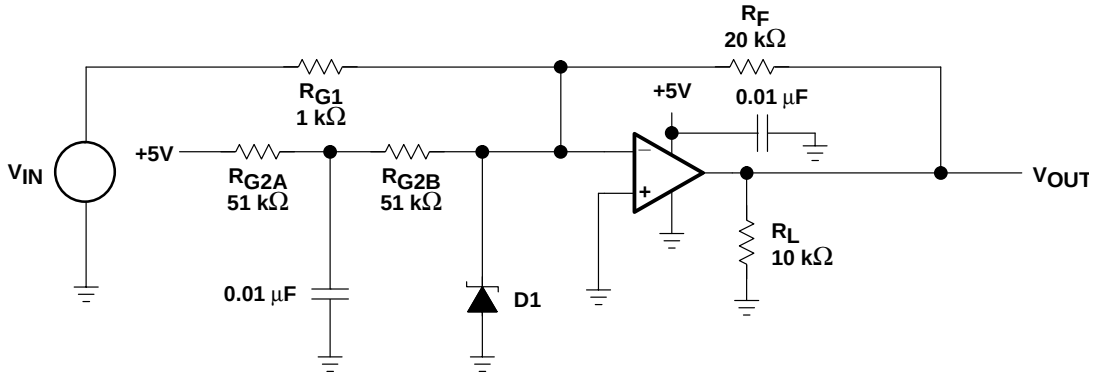


Figure 4–20. Case 4 Example Circuit

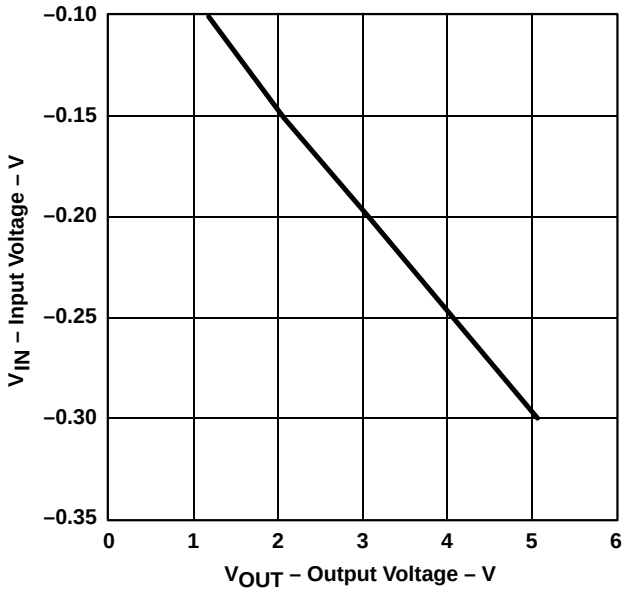


Figure 4–21. Case 4 Example Circuit Measured Transfer Curve

The TLV247X was used to build the test circuit because of its wide dynamic range. The transfer curve plots very close to the theoretical curve, and this results from using a high performance op amp.

As long as the circuit works normally there are no problems handling the negative voltage input to the circuit because the inverting lead of the TLV247X is at a positive voltage. The positive op amp input lead is grounded, and normal op amp operation keeps the inverting op amp input lead at ground because of the assumption that the error voltage is zero. When V_{CC} is powered down while there is a negative voltage on the inverting op amp input lead.

The most prudent solution is to connect the diode, D_1, with its cathode on the inverting op amp input lead and its anode at ground. If a negative voltage gets on the inverting op amp input lead it is clamped to ground by the diode. Select the diode type as germanium or Schottky so the voltage drop across the diode is about 200 mV; this small voltage does not harm most op amp inputs. R_{G2} is split into two resistors ($R_{G2A} = R_{G2B} = 51\ k\Omega$) with a capacitor inserted at the junction of the two resistors. This places a power supply filter in series with V_{CC}.

4.4 Summary

Single-supply op amp design is more complicated than split-supply op amp design, but with a logical design approach excellent results are achieved. Single-supply design used to be considered technically limiting because older op amps had limited capability. The new op amps, such as the TLC247X, TLC07X, and TLC08X have excellent single-supply parameters; thus when used in the correct applications these op amps yield rail-to-rail performance equal to their split-supply counterparts.

Single-supply op amp design usually involves some form of biasing, and this requires more thought, so single-supply op amp design needs discipline and a procedure. The recommended design procedure for single-supply op amp design is:

- Substitute the specification data into simultaneous equations to obtain m and b (the slope and intercept of a straight line).
- Let m and b determine the form of the circuit.
- Choose the circuit configuration that fits the form.
- Using the circuit equations for the circuit configuration selected, calculate the resistor values.
- Build the circuit, take data, and verify performance.
- Test the circuit for nonstandard operating conditions (circuit power off while interface power is on, over/under range inputs, etc.).
- Add protection components as required.
- Retest.

When this procedure is followed, good results follow. As single-supply circuit designers expand their horizon, new challenges require new solutions. Remember, the only equation a linear op amp can produce is the equation of a straight line. That equation only has four forms. The new challenges may consist of multiple inputs, common-mode voltage rejection, or something different, but this method can be expanded to meet these challenges.

Chapter 5

Feedback and Stability Theory

Ron Mancini

5.1 Why Study Feedback Theory?

The gain of all op amps decreases as frequency increases, and the decreasing gain results in decreasing accuracy as the ideal op amp assumption ($a \Rightarrow \infty$) breaks down. In most real op amps the open loop gain starts to decrease before 10 Hz, so an understanding of feedback is required to predict the closed loop performance of the op amp. The real world application of op amps is feedback controlled, and depends on op amp open loop gain at a given frequency. A designer must know theory to be able to predict the circuit response regardless of frequency or open loop gain.

Analysis tools have something in common with medicine because they both can be distasteful but necessary. Medicine often tastes bad or has undesirable side effects, and analysis tools involve lots of hard learning work before they can be applied to yield results. Medicine assists the body in fighting an illness; analysis tools assist the brain in learning/designing feedback circuits.

The analysis tools given here are a synopsis of salient points; thus they are detailed enough to get you where you are going without any extras. The references, along with thousands of their counterparts, must be consulted when making an in-depth study of the field. Aspirin, home remedies, and good health practice handle the majority of health problems, and these analysis tools solve the majority of circuit problems.

Ideal op amp circuits can be designed without knowledge of feedback analysis tools, but these circuits are limited to low frequencies. Also, an understanding of feedback analysis tools is required to understand AC effects like ringing and oscillations.

5.2 Block Diagram Math and Manipulations

Electronic systems and circuits are often represented by block diagrams, and block diagrams have a unique algebra and set of transformations[1]. Block diagrams are used because they are a shorthand pictorial representation of the cause-and-effect relationship between the input and output in a real system. They are a convenient method for characterizing the functional relationships between components. It is not necessary to understand the functional details of a block to manipulate a block diagram.

The input impedance of each block is assumed to be infinite to preclude loading. Also, the output impedance of each block is assumed to be zero to enable high fan-out. The systems designer sets the actual impedance levels, but the fan-out assumption is valid because the block designers adhere to the system designer's specifications. All blocks multiply the input times the block quantity (see Figure 5–1) unless otherwise specified within the block. The quantity within the block can be a constant as shown in Figure 5–1(c), or it can be a complex math function involving Laplace transforms. The blocks can perform time-based operations such as differentiation and integration.

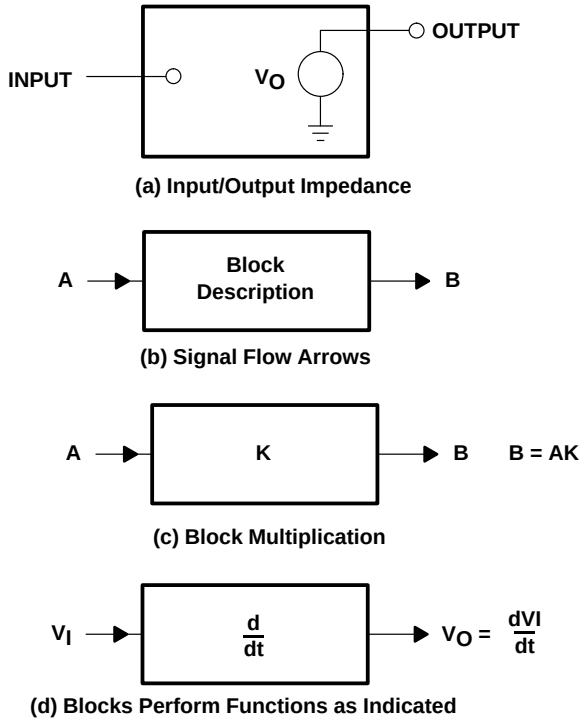


Figure 5–1. Definition of Blocks

Adding and subtracting are done in special blocks called summing points. Figure 5–2 gives several examples of summing points. Summing points can have unlimited inputs, can add or subtract, and can have mixed signs yielding addition and subtraction within a single summing point. Figure 5–3 defines the terms in a typical control system, and Figure 5–4 defines the terms in a typical electronic feedback system. Multiloop feedback systems (Figure 5–5) are intimidating, but they can be reduced to a single loop feedback system, as shown in the figure, by writing equations and solving for V_{OUT}/V_{IN}. An easier method for reducing multiloop feedback systems to single loop feedback systems is to follow the rules and use the transforms given in Figure 5–6.

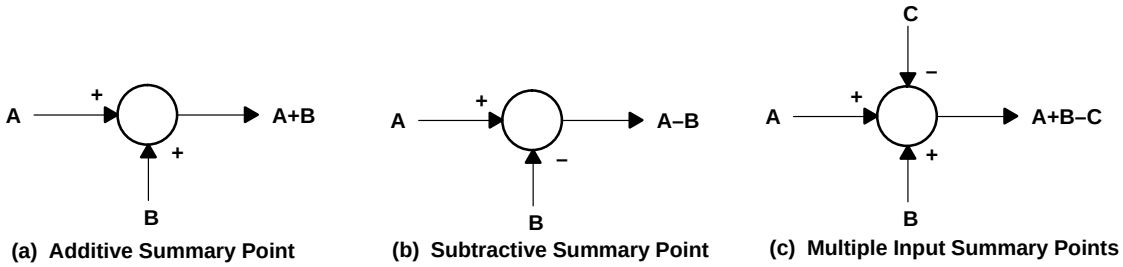


Figure 5–2. Summary Points

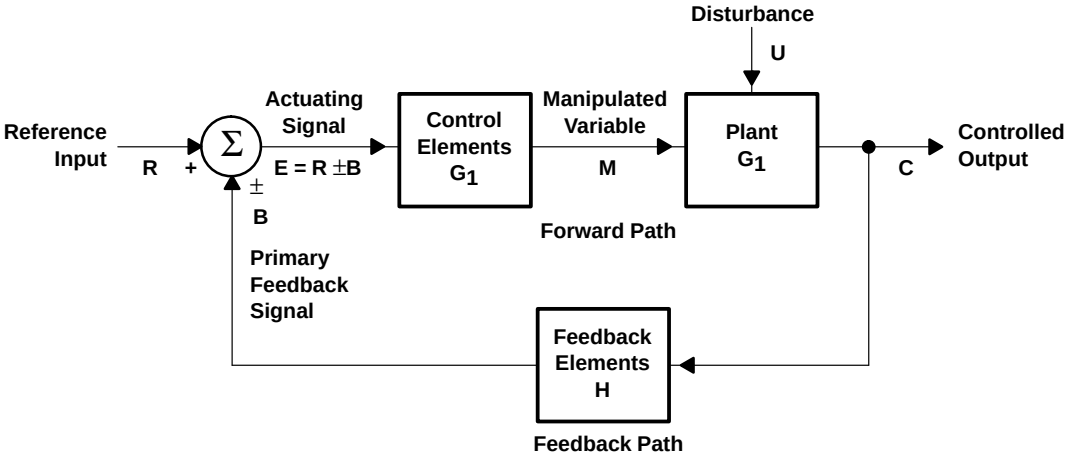


Figure 5–3. Definition of Control System Terms

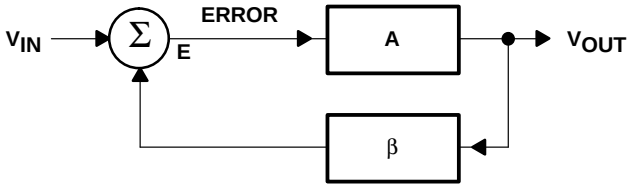


Figure 5–4. Definition of an Electronic Feedback Circuit

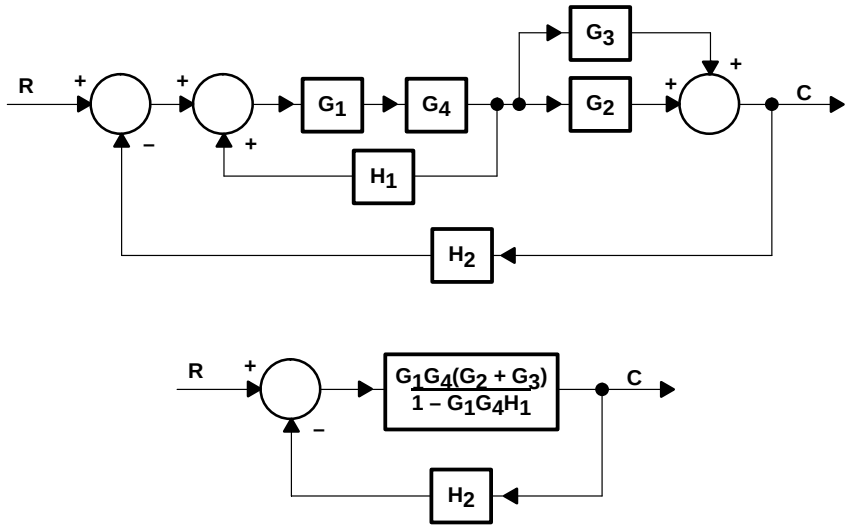


Figure 5–5. Multiloop Feedback System

Block diagram reduction rules:

- Combine cascade blocks.
- Combine parallel blocks.
- Eliminate interior feedback loops.
- Shift summing points to the left.
- Shift takeoff points to the right.
- Repeat until canonical form is obtained.

Figure 5–6 gives the block diagram transforms. The idea is to reduce the diagram to its canonical form because the canonical feedback loop is the simplest form of a feedback loop, and its analysis is well documented. All feedback systems can be reduced to the canonical form, so all feedback systems can be analyzed with the same math. A canonical loop exists for each input to a feedback system; although the stability dynamics are independent of the input, the output results are input dependent. The response of each input of a multiple input feedback system can be analyzed separately and added through superposition.

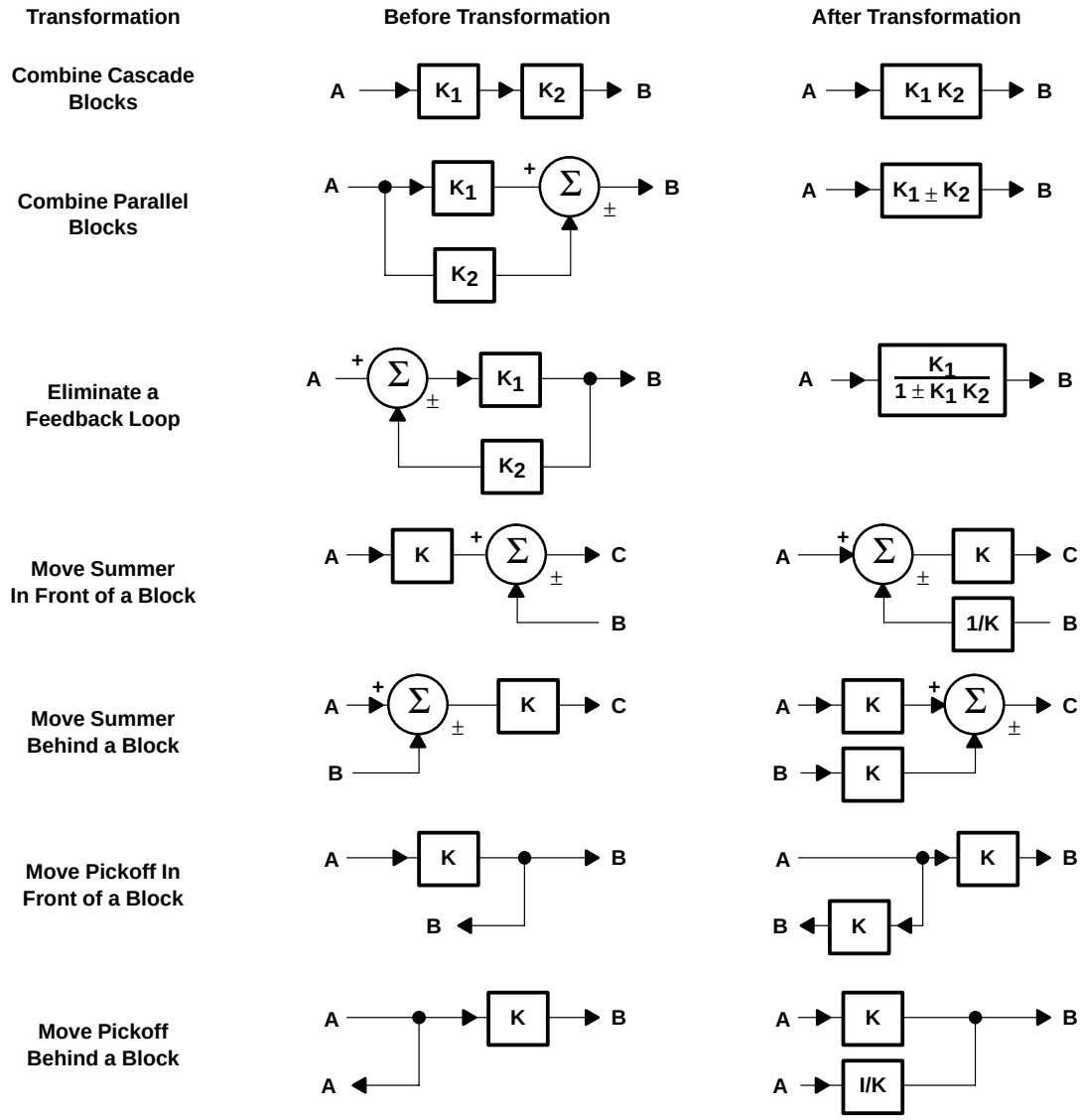


Figure 5–6. Block Diagram Transforms

5.3 Feedback Equation and Stability

Figure 5–7 shows the canonical form of a feedback loop with control system and electronic system terms. The terms make no difference except that they have meaning to the system engineers, but the math does have meaning, and it is identical for both types of terms. The electronic terms and negative feedback sign are used in this analysis, because subsequent chapters deal with electronic applications. The output equation is written in Equation 5–1.

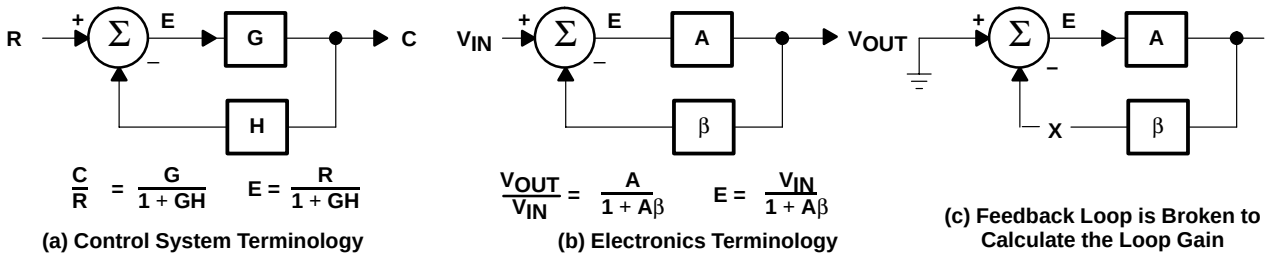


Figure 5–7. Comparison of Control and Electronic Canonical Feedback Systems

$$V_{OUT} = EA \tag{5–1}$$

The error equation is written in Equation 5–2.

$$E = V_{IN} - \beta V_{OUT} \tag{5–2}$$

Combining Equations 5–1 and 5–2 yields Equation 5–3.

$$\frac{V_{OUT}}{A} = V_{IN} - \beta V_{OUT} \tag{5–3}$$

Collecting terms yields Equation 5–4.

$$V_{OUT}\left(\frac{1}{A} + \beta\right) = V_{IN} \tag{5–4}$$

Rearranging terms yields the classic form of the feedback Equation 5–5.

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \tag{5–5}$$

When the quantity $A\beta$ in Equation 5–5 becomes very large with respect to one, the one can be neglected, and Equation 5–5 reduces to Equation 5–6, which is the ideal feedback equation. Under the conditions that $A\beta >> 1$, the system gain is determined by the feedback factor β. Stable passive circuit components are used to implement the feedback factor, thus in the ideal situation, the closed loop gain is predictable and stable because β is predictable and stable.

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{\beta} \tag{5–6}$$

The quantity Aβ is so important that it has been given a special name: loop gain. In Figure 5–7, when the voltage inputs are grounded (current inputs are opened) and the loop is broken, the calculated gain is the loop gain, Aβ. Now, keep in mind that we are using complex numbers, which have magnitude and direction. When the loop gain approaches minus one, or to express it mathematically $1\angle -180°$, Equation 5–5 approaches $1/0 \Rightarrow \propto$. The circuit output heads for infinity as fast as it can using the equation of a straight line. If the output were not energy limited, the circuit would explode the world, but happily, it is energy limited, so somewhere it comes up against the limit.

Active devices in electronic circuits exhibit nonlinear phenomena when their output approaches a power supply rail, and the nonlinearity reduces the gain to the point where the loop gain no longer equals $1\angle -180°$. Now the circuit can do two things: first it can become stable at the power supply limit, or second, it can reverse direction (because stored charge keeps the output voltage changing) and head for the negative power supply rail.

The first state where the circuit becomes stable at a power supply limit is named lockup; the circuit will remain in the locked up state until power is removed and reapplied. The second state where the circuit bounces between power supply limits is named oscillatory. Remember, the loop gain, Aβ, is the sole factor determining stability of the circuit or system. Inputs are grounded or disconnected, so they have no bearing on stability.

Equations 5–1 and 5–2 are combined and rearranged to yield Equation 5–7, which is the system or circuit error equation.

$$E = \frac{V_{IN}}{1 + A\beta} \tag{5–7}$$

First, notice that the error is proportional to the input signal. This is the expected result because a bigger input signal results in a bigger output signal, and bigger output signals require more drive voltage. As the loop gain increases, the error decreases, thus large loop gains are attractive for minimizing errors.

5.4 Bode Analysis of Feedback Circuits

H. W. Bode developed a quick, accurate, and easy method of analyzing feedback amplifiers, and he published a book about his techniques in 1945.[2] Operational amplifiers had not been developed when Bode published his book, but they fall under the general classification of feedback amplifiers, so they are easily analyzed with Bode techniques. The mathematical manipulations required to analyze a feedback circuit are complicated because they involve multiplication and division. Bode developed the Bode plot, which simplifies the analysis through the use of graphical techniques.

The Bode equations are log equations that take the form 20LOG(F(t)) = 20LOG(|F(t)|) + phase angle. Terms that are normally multiplied and divided can now be added and subtracted because they are log equations. The addition and subtraction is done graphically, thus easing the calculations and giving the designer a pictorial representation of circuit performance. Equation 5–8 is written for the low pass filter shown in Figure 5–8.

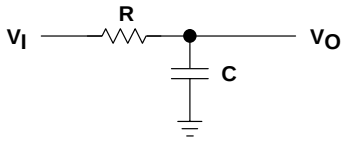


Figure 5–8. Low-Pass Filter

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{1}{C\,s}}{R + \frac{1}{C\,s}} = \frac{1}{1 + RCs} = \frac{1}{1 + \tau s} \qquad (5\text{–}8)$$

Where: $s = j\omega$, $j = \sqrt{(-1)}$, and $RC = \tau$

The magnitude of this transfer function is $|V_{OUT}/V_{IN}| = 1/\sqrt{1^2 + (\tau\omega)^2}$. This magnitude, $|V_{OUT}/V_{IN}| \cong 1$ when $\omega = 0.1/\tau$, it equals 0.707 when $\omega = 1/\tau$, and it is approximately = 0.1 when $\omega = 10/\tau$. These points are plotted in Figure 5–9 using straight line approximations. The negative slope is –20 dB/decade or –6 dB/octave. The magnitude curve is plotted as a horizontal line until it intersects the breakpoint where $\omega = 1/\tau$. The negative slope begins at the breakpoint because the magnitude starts decreasing at that point. The gain is equal to 1 or 0 dB at very low frequencies, equal to 0.707 or –3 dB at the break frequency, and it keeps falling with a –20 dB/decade slope for higher frequencies.

The phase shift for the low pass filter or any other transfer function is calculated with the aid of Equation 5–9.

$$\phi = \text{tangent}^{-1}\left(\frac{\text{Real}}{\text{Imaginary}}\right) = -\text{tangent}^{-1}\left(\frac{\omega\tau}{1}\right) \qquad (5\text{–}9)$$

The phase shift is much harder to approximate because the tangent function is nonlinear. Normally the phase information is only required around the 0 dB intercept point for an active circuit, so the calculations are minimized. The phase is shown in Figure 5–9, and it is approximated by remembering that the tangent of 90° is 1, the tangent of 60° is $\sqrt{3}$, and the tangent of 30° is $\sqrt{3}/3$.

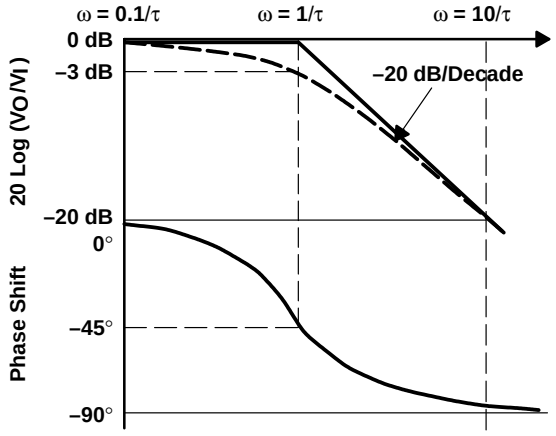


Figure 5–9. Bode Plot of Low-Pass Filter Transfer Function

A breakpoint occurring in the denominator is called a pole, and it slopes down. Conversely, a breakpoint occurring in the numerator is called a zero, and it slopes up. When the transfer function has multiple poles and zeros, each pole or zero is plotted independently, and the individual poles/zeros are added graphically. If multiple poles, zeros, or a pole/zero combination have the same breakpoint, they are plotted on top of each other. Multiple poles or zeros cause the slope to change by multiples of 20 dB/decade.

An example of a transfer function with multiple poles and zeros is a band reject filter (see Figure 5–10). The transfer function of the band reject filter is given in Equation 5–10.

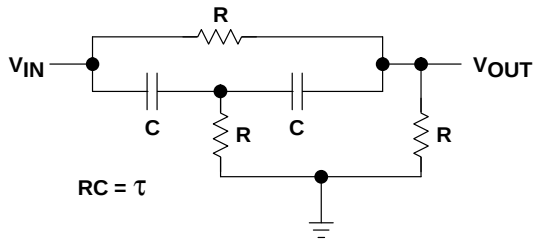


Figure 5–10. Band Reject Filter

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{(1 + \tau s)(1 + \tau s)}{2\left(1 + \frac{\tau s}{0.44}\right)\left(1 + \frac{\tau s}{4.56}\right)} \qquad (5\text{–}10)$$

The pole zero plot for each individual pole and zero is shown in Figure 5–11, and the combined pole zero plot is shown in Figure 5–12.

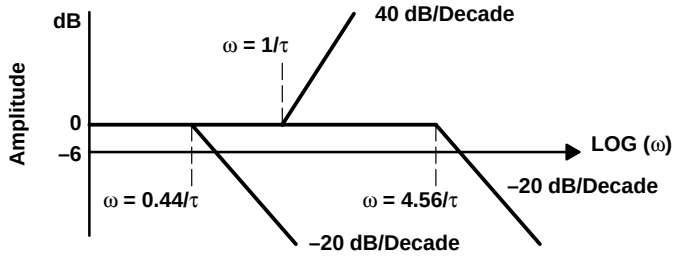


Figure 5–11. Individual Pole Zero Plot of Band Reject Filter

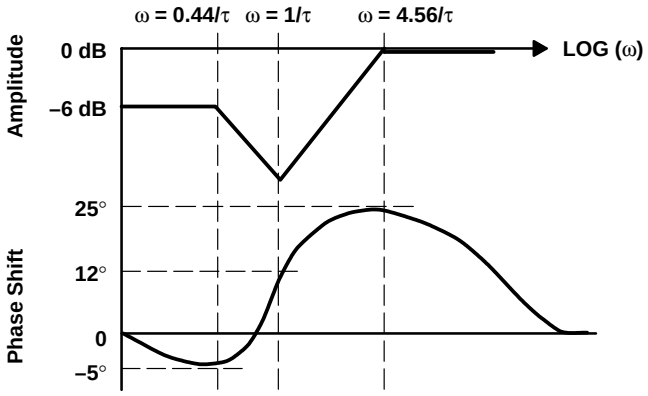


Figure 5–12. Combined Pole Zero Plot of Band Reject Filter

The individual pole zero plots show the dc gain of 1/2 plotting as a straight line from the –6 dB intercept. The two zeros occur at the same break frequency, thus they add to a 40-dB/decade slope. The two poles are plotted at their breakpoints of $\omega = 0.44/\tau$ and $\omega = 4.56/\tau$. The combined amplitude plot intercepts the amplitude axis at –6 dB because of the dc gain, and then breaks down at the first pole. When the amplitude function gets to the double zero, the first zero cancels out the first pole, and the second zero breaks up. The upward slope continues until the second pole cancels out the second zero, and the amplitude is flat from that point out in frequency.

When the separation between all the poles and zeros is great, a decade or more in frequency, it is easy to draw the Bode plot. As the poles and zeros get closer together, the plot gets harder to make. The phase is especially hard to plot because of the tangent function, but picking a few salient points and sketching them in first gets a pretty good approximation.[3] The Bode plot enables the designer to get a good idea of pole zero placement, and it is valuable for fast evaluation of possible compensation techniques. When the situation gets critical, accurate calculations must be made and plotted to get an accurate result.

Consider Equation 5–11.

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \tag{5–11}$$

Taking the log of Equation 5–11 yields Equation 5–12.

$$20\text{Log}\left(\frac{V_{OUT}}{V_{IN}}\right) = 20\text{Log}(A) - 20\text{Log}(1 + A\beta) \tag{5–12}$$

If A and β do not contain any poles or zeros there will be no break points. Then the Bode plot of Equation 5–12 looks like that shown in Figure 5–13, and because there are no poles to contribute negative phase shift, the circuit cannot oscillate.

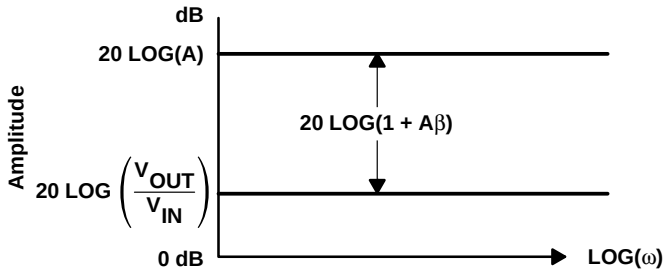


Figure 5–13. When No Pole Exists in Equation (5–12)

All real amplifiers have many poles, but they are normally internally compensated so that they appear to have a single pole. Such an amplifier would have an equation similar to that given in Equation 5–13.

$$A = \frac{a}{1 + j\frac{\omega}{\omega_a}} \tag{5–13}$$

The plot for the single pole amplifier is shown in Figure 5–14.

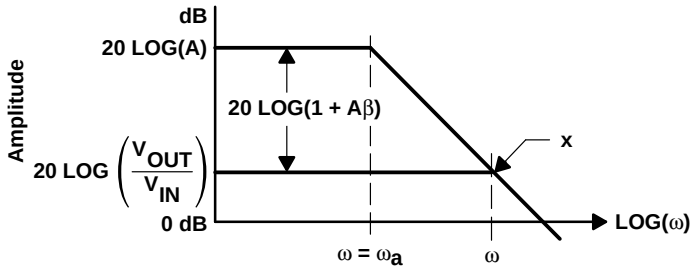


Figure 5–14. When Equation 5–12 has a Single Pole

The amplifier gain, A, intercepts the amplitude axis at 20Log(A), and it breaks down at a slope of –20 dB/decade at $\omega = \omega_a$. The negative slope continues for all frequencies greater than the breakpoint, $\omega = \omega_a$. The closed loop circuit gain intercepts the amplitude axis at $20\text{Log}(V_{OUT}/V_{IN})$, and because β does not have any poles or zeros, it is constant until its projection intersects the amplifier gain at point X. After intersection with the amplifier gain curve, the closed loop gain follows the amplifier gain because the amplifier is the controlling factor.

Actually, the closed loop gain starts to roll off earlier, and it is down 3 dB at point X. At point X the difference between the closed loop gain and the amplifier gain is –3 dB, thus according to Equation 5–12 the term $-20\text{Log}(1+A\beta) = -3$ dB. The magnitude of 3 dB is $\sqrt{2}$, hence $\sqrt{1 + (A\beta)^2} = \sqrt{2}$, and elimination of the radicals shows that $A\beta = 1$. There is a method [4] of relating phase shift and stability to the slope of the closed loop gain curves, but only the Bode method is covered here. An excellent discussion of poles, zeros, and their interaction is given by M. E Van Valkenberg,[5] and he also includes some excellent prose to liven the discussion.

5.5 Loop Gain Plots are the Key to Understanding Stability

Stability is determined by the loop gain, and when $A\beta = -1 = |1| \angle -180°$ instability or oscillation occurs. If the magnitude of the gain exceeds one, it is usually reduced to one by circuit nonlinearities, so oscillation generally results for situations where the gain magnitude exceeds one.

Consider oscillator design, which depends on nonlinearities to decrease the gain magnitude; if the engineer designed for a gain magnitude of one at nominal circuit conditions, the gain magnitude would fall below one under worst case circuit conditions causing oscillation to cease. Thus, the prudent engineer designs for a gain magnitude of one under worst case conditions knowing that the gain magnitude is much more than one under optimistic conditions. The prudent engineer depends on circuit nonlinearities to reduce the gain magnitude to the appropriate value, but this same engineer pays a price of poorer distortion performance. Sometimes a design compromise is reached by putting a nonlinear component, such as a lamp, in the feedback loop to control the gain without introducing distortion.

Some high gain control systems always have a gain magnitude greater than one, but they avoid oscillation by manipulating the phase shift. The amplifier designer who pushes the amplifier for superior frequency performance has to be careful not to let the loop gain phase shift accumulate to 180°. Problems with overshoot and ringing pop up before the loop gain reaches 180° phase shift, thus the amplifier designer must keep a close eye on loop dynamics. Ringing and overshoot are handled in the next section, so preventing oscillation is emphasized in this section. Equation 5–14 has the form of many loop gain transfer functions or circuits, so it is analyzed in detail.

$$(A)\beta = \frac{(K)}{\left(1 + \tau_1(s)\right)\left(1 + \tau_2(s)\right)} \tag{5–14}$$

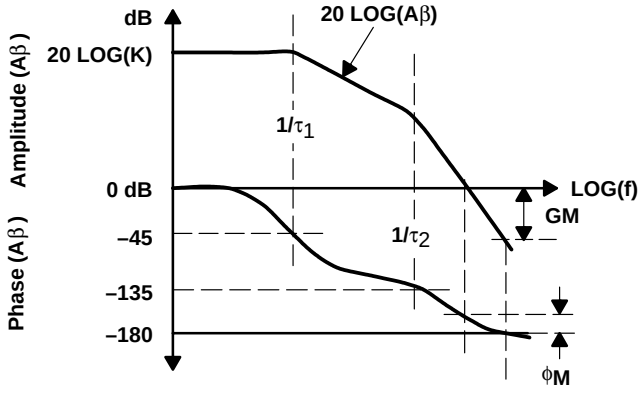


Figure 5–15. Magnitude and Phase Plot of Equation 5–14

The quantity, K, is the dc gain, and it plots as a straight line with an intercept of 20Log(K). The Bode plot of Equation 5–14 is shown in Figure 5–15. The two break points, $\omega = \omega_1 = 1/\tau_1$ and $\omega = \omega_2 = 1/\tau_2$, are plotted in the Bode plot. Each breakpoint adds –20 dB/decade slope to the plot, and 45° phase shift accumulates at each breakpoint. This transfer function is referred to as a two slope because of the two breakpoints. The slope of the curve when it crosses the 0 dB intercept indicates phase shift and the ability to oscillate. Notice that a one slope can only accumulate 90° phase shift, so when a transfer function passes through 0 dB with a one slope, it cannot oscillate. Furthermore, a two-slope system can accumulate 180° phase shift, therefore a transfer function with a two or greater slope is capable of oscillation.

A one slope crossing the 0 dB intercept is stable, whereas a two or greater slope crossing the 0 dB intercept may be stable or unstable depending upon the accumulated phase shift. Figure 5–15 defines two stability terms; the phase margin, ϕ_M, and the gain margin, G_M. Of these two terms the phase margin is much more important because phase shift is critical for stability. Phase margin is a measure of the difference in the actual phase shift and the theoretical 180° required for oscillation, and the phase margin measurement or calculation is made at the 0 dB crossover point. The gain margin is measured or calculated at the 180° phase crossover point. Phase margin is expressed mathematically in Equation 5–15.

$$\phi_M = 180 - \text{tangent}^{-1}(A\beta) \tag{5–15}$$

The phase margin in Figure 5–15 is very small, 20°, so it is hard to measure or predict from the Bode plot. A designer probably doesn't want a 20° phase margin because the system overshoots and rings badly, but this case points out the need to calculate small phase margins carefully. The circuit is stable, and it does not oscillate because the phase margin is positive. Also, the circuit with the smallest phase margin has the highest frequency response and bandwidth.

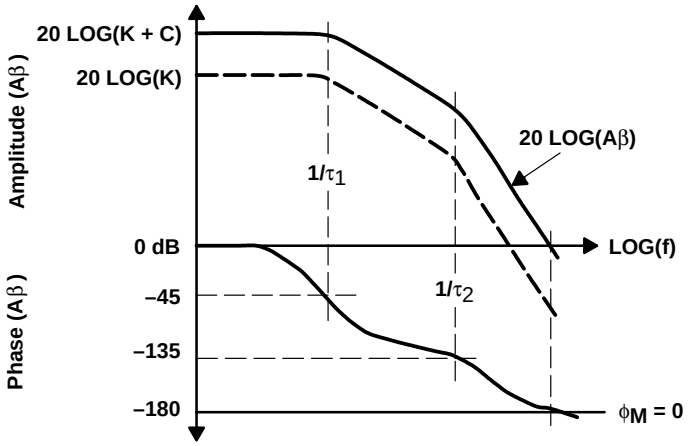


Figure 5–16. Magnitude and Phase Plot of the Loop Gain Increased to (K+C)

Increasing the loop gain to (K+C) as shown in Figure 5–16 shifts the magnitude plot up. If the pole locations are kept constant, the phase margin reduces to zero as shown, and the circuit will oscillate. The circuit is not good for much in this condition because production tolerances and worst case conditions ensure that the circuit will oscillate when you want it to amplify, and vice versa.

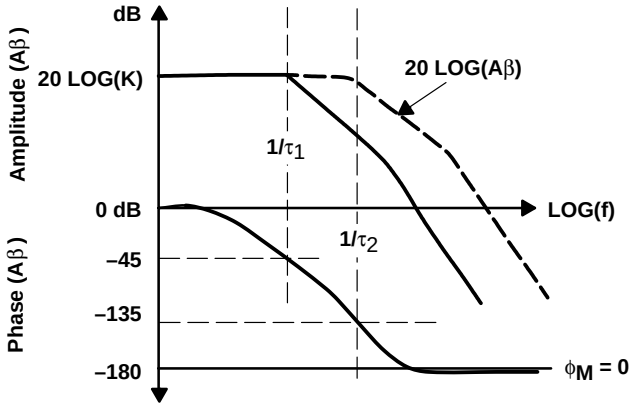


Figure 5–17. Magnitude and Phase Plot of the Loop Gain With Pole Spacing Reduced

The circuit poles are spaced closer in Figure 5–17, and this results in a faster accumulation of phase shift. The phase margin is zero because the loop gain phase shift reaches 180° before the magnitude passes through 0 dB. This circuit oscillates, but it is not a very stable oscillator because the transition to 180° phase shift is very slow. Stable oscillators have a very sharp transition through 180°.

When the closed loop gain is increased the feedback factor, β, is decreased because $V_{OUT}/V_{IN} = 1/\beta$ for the ideal case. This in turn decreases the loop gain, $A\beta$, thus the stability increases. In other words, increasing the closed loop gain makes the circuit more stable. Stability is not important except to oscillator designers because overshoot and ringing become intolerable to linear amplifiers long before oscillation occurs. The overshoot and ringing situation is investigated next.

5.6 The Second Order Equation and Ringing/Overshoot Predictions

The second order equation is a common approximation used for feedback system analysis because it describes a two-pole circuit, which is the most common approximation used. All real circuits are more complex than two poles, but except for a small fraction, they can be represented by a two-pole equivalent. The second order equation is extensively described in electronic and control literature [6].

$$(1 + A\beta) = 1 + \frac{K}{(1 + \tau_1 s)(1 + \tau_2 s)} \tag{5–16}$$

After algebraic manipulation Equation 5–16 is presented in the form of Equation 5–17.

$$s^2 + S\frac{\tau_1 + \tau_2}{\tau_1 \tau_2} + \frac{1 + K}{\tau_1 \tau_2} = 0 \tag{5–17}$$

Equation 5–17 is compared to the second order control Equation 5–18, and the damping ratio, ζ, and natural frequency, w_N are obtained through like term comparisons.

$$s^2 + 2\zeta\omega_N s + \omega_N^2 \tag{5–18}$$

Comparing these equations yields formulas for the phase margin and per cent overshoot as a function of damping ratio.

$$\omega_N = \sqrt{\frac{1 + K}{\tau_1 \tau_2}} \tag{5–19}$$

$$\xi = \frac{\tau_1 + \tau_2}{2\omega_N \tau_1 \tau_2} \tag{5–20}$$

When the two poles are well separated, Equation 5–21 is valid.

$$\phi_M = \text{tangent}^{-1}(2\xi) \tag{5–21}$$

The salient equations are plotted in Figure 5–18, which enables a designer to determine the phase margin and overshoot when the gain and pole locations are known.

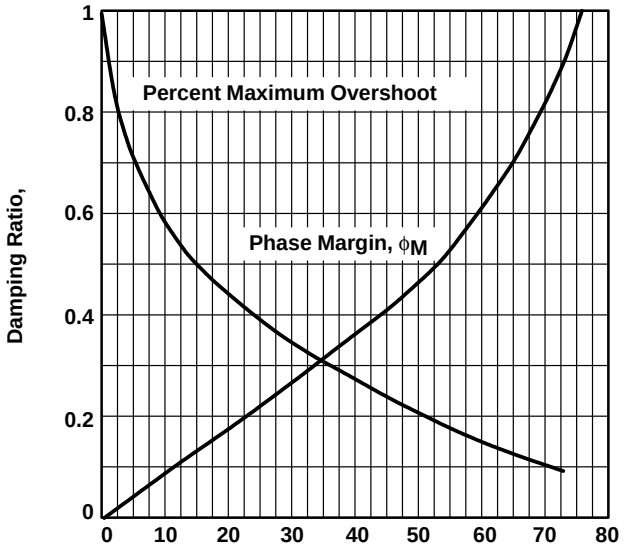


Figure 5–18. Phase Margin and Overshoot vs Damping Ratio

Enter Figure 5–18 at the calculated damping ratio, say 0.4, and read the overshoot at 25% and the phase margin at 42°. If a designer had a circuit specification of 5% maximum overshoot, then the damping ratio must be 0.78 with a phase margin of 62°.

5.7 References

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Chapter 6

Development of the Non Ideal Op Amp Equations

Ron Mancini

6.1 Introduction

There are two types of error sources in op amps, and they fall under the general classification of dc and ac errors. Examples of dc errors are input offset voltage and input bias current. The dc errors stay constant over the usable op amp frequency range; therefore, the input bias current is 10 pA at 1 kHz and it is 10 pA at 10 kHz. Because of their constant and controlled behavior, dc errors are not considered until later chapters.

AC errors are flighty, so we address them here by developing a set of nonideal equations that account for ac errors. The ac errors may show up under dc conditions, but they get worse as the operating frequency increases. A good example of an ac error is common–mode rejection ration (CMRR). Most op amps have a guaranteed CMRR specification, but this specification is only valid at dc or very low frequencies. Further inspection of the data sheet reveals that CMRR decreases as operating frequency increases. Several other specifications that fall into the category of ac specifications are output impedance, power-supply rejection-ratio, peak-to-peak output voltage, differential gain, differential phase, and phase margin.

Differential gain is the most important ac specification because the other ac specifications are derived from the differential gain. Until now, differential gain has been called op amp gain or op amp open loop gain, and we shall continue with that terminology. Let the data sheet call it differential gain.

As shown in prior chapters, when frequency increases, the op amp gain decreases and errors increase. This chapter develops the equations that illustrate the effects of the gain changes. We start with a review of the basic canonical feedback system stability because the op amp equations are developed using the same techniques.

Amplifiers are built with active components such as transistors. Pertinent transistor parameters like transistor gain are subject to drift and initial inaccuracies from many sources, so amplifiers being built from these components are subject to drift and inaccura-

cies. The drift and inaccuracy is minimized or eliminated by using negative feedback. The op amp circuit configuration employs feedback to make the transfer equation of the circuit independent of the amplifier parameters (well almost), and while doing this, the circuit transfer function is made dependent on external passive components. The external passive components can be purchased to meet almost any drift or accuracy specification; only the cost and size of the passive components limit their use.

Once feedback is applied to the op amp it is possible for the op amp circuit to become unstable. Certain amplifiers belong to a family called internally compensated op amps; they contain internal capacitors that are sometimes advertised as precluding instabilities. Although internally compensated op amps should not oscillate when operated under specified conditions, many have relative stability problems that manifest themselves as poor phase response, ringing, and overshoot. The only absolutely stable internally compensated op amp is the one lying on the workbench without power applied! All other internally compensated op amps oscillate under some external circuit conditions.

Noninternally compensated or *externally* compensated op amps are unstable without the addition of external stabilizing components. This situation is a disadvantage in many cases because they require additional components, but the lack of internal compensation enables the top-drawer circuit designer to squeeze the last drop of performance from the op amp. You have two options: op amps internally compensated by the IC manufacturer, or op amps externally compensated by you. Compensation, except that done by the op amp manufacturer, must be done external to the IC. Surprisingly enough, internally compensated op amps require external compensation for demanding applications.

Compensation is achieved by adding external components that modify the circuit transfer function so that it becomes unconditionally stable. There are several different methods of compensating an op amp, and as you might suspect, there are pros and cons associated with each method of compensation. After the op amp circuit is compensated, it must be analyzed to determine the effects of compensation. The modifications that compensation have on the closed loop transfer function often determine which compensation scheme is most profitably employed.

6.2 Review of the Canonical Equations

A block diagram for a generalized feedback system is repeated in Figure 6–1. This simple block diagram is sufficient to determine the stability of any system.

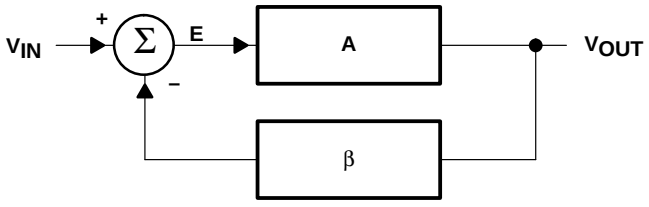

Figure 6–1. Feedback System Block Diagram

The output and error equation development is repeated below.

$$V_{OUT} = EA \tag{6–1}$$

$$E = V_{IN} - \beta V_{OUT} \tag{6–2}$$

Combining Equations 6–1 and 6–2 yields Equation 6–3:

$$\frac{V_{OUT}}{A} = V_{IN} - \beta V_{OUT} \tag{6–3}$$

Collecting terms yields Equation 6–4:

$$V_{OUT}\left(\frac{1}{A} + \beta\right) = V_{IN} \tag{6–4}$$

Rearranging terms yields the classic form of the feedback equation.

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \tag{6–5}$$

Notice that Equation 6–5 reduces to Equation 6–6 when the quantity Aβ in Equation 6–5 becomes very large with respect to one. Equation 6–6 is called the ideal feedback equation because it depends on the assumption that Aβ >> 1, and it finds extensive use when amplifiers are assumed to have ideal qualities. Under the conditions that Aβ >>1, the system gain is determined by the feedback factor β. Stable passive circuit components are used to implement the feedback factor, thus the ideal closed loop gain is predictable and stable because β is predictable and stable.

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{\beta} \tag{6–6}$$

The quantity Aβ is so important that it has been given a special name, loop gain. Consider Figure 6–2; when the voltage inputs are grounded (current inputs are opened) and the loop is broken, the calculated gain is the loop gain, Aβ. Now, keep in mind that this is a mathematics of complex numbers, which have magnitude and direction. When the loop gain approaches minus one, or to express it mathematically $1 \angle -180°$, Equation 6–5 approaches infinity because $1/0 \Rightarrow \infty$. The circuit output heads for infinity as fast as it can

using the equation of a straight line. If the output were not energy limited the circuit would explode the world, but it is energy limited by the power supplies so the world stays intact.

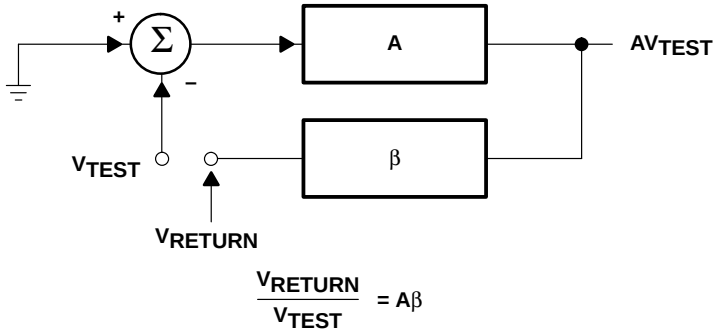

Figure 6–2. Feedback Loop Broken to Calculate Loop Gain

Active devices in electronic circuits exhibit nonlinear behavior when their output approaches a power supply rail, and the nonlinearity reduces the amplifier gain until the loop gain no longer equals $1\angle -180°$. Now the circuit can do two things: first, it could become stable at the power supply limit, or second, it can reverse direction (because stored charge keeps the output voltage changing) and head for the negative power supply rail.

The first state where the circuit becomes stable at a power supply limit is named lockup; the circuit will remain in the locked up state until power is removed. The second state where the circuit bounces between power supply limits is named oscillatory. Remember, the loop gain, $A\beta$, is the sole factor that determines stability for a circuit or system. Inputs are grounded or disconnected when the loop gain is calculated, so they have no effect on stability. The loop gain criteria is analyzed in depth later.

Equations 6–1 and 6–2 are combined and rearranged to yield Equation 6–7, which gives an indication of system or circuit error.

$$E = \frac{V_{IN}}{1 + A\beta} \tag{6–7}$$

First, notice that the error is proportional to the input signal. This is the expected result because a bigger input signal results in a bigger output signal, and bigger output signals require more drive voltage. Second, the loop gain is inversely proportional to the error. As the loop gain increases the error decreases, thus large loop gains are attractive for minimizing errors. Large loop gains also decrease stability, thus there is always a tradeoff between error and stability.

6.3 Noninverting Op Amps

A noninverting op amp is shown in Figure 6–3. The dummy variable, V_B, is inserted to make the calculations easier and a is the op amp gain.

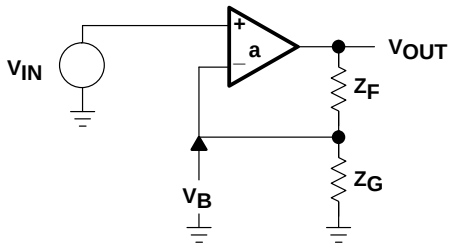

Figure 6–3. Noninverting Op Amp

Equation 6–8 is the amplifier transfer equation.

$$V_{OUT} = a\left(V_{IN} - V_B\right) \tag{6–8}$$

The output equation is developed with the aid of the voltage divider rule. Using the voltage divider rule assumes that the op amp impedance is low.

$$V_B = \frac{V_{OUT} Z_G}{Z_F + Z_G} \text{ for } I_B = 0 \tag{6–9}$$

Combining Equations 6–8 and 6–9 yields Equation 6–10.

$$V_{OUT} = aV_{IN} - \frac{aZ_G V_{OUT}}{Z_G + Z_F} \tag{6–10}$$

Rearranging terms in Equation 6–10 yields Equation 6–11, which describes the transfer function of the circuit.

$$\frac{V_{OUT}}{V_{IN}} = \frac{a}{1 + \frac{aZ_G}{Z_G + Z_F}} \tag{6–11}$$

Equation 6–5 is repeated as Equation 6–12 to make a term by term comparison of the equations easy.

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \tag{6–12}$$

By virtue of the comparison we get Equation 6–13, which is the loop-gain equation for the noninverting op amp. The loop-gain equation determines the stability of the circuit. The

comparison also shows that the open loop gain, A, is equal to the op amp open loop gain, a, for the noninverting circuit.

$$A\beta = \frac{aZ_G}{Z_G + Z_F} \tag{6–13}$$

Equation 6–13 is also derived with the aid of Figure 6–4, which shows the open loop noninverting op amp.

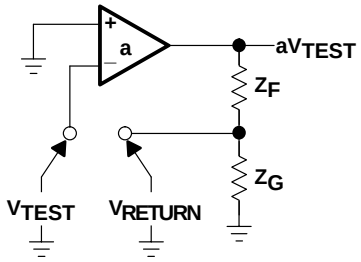

Figure 6–4. Open Loop Noninverting Op Amp

The test voltage, V_{TEST}, is multiplied by the op amp open loop gain to obtain the op amp output voltage, aV_{TEST}. The voltage divider rule is used to calculate Equation 6–15, which is identical to Equation 6–14 after some algebraic manipulation.

$$V_{RETURN} = \frac{aV_{TEST}\,Z_G}{Z_F + Z_G} \tag{6–14}$$

$$\frac{V_{RETURN}}{V_{TEST}} = A\beta = \frac{aZ_G}{Z_F + Z_G} \tag{6–15}$$

6.4 Inverting Op Amps

The inverting op amp circuit is shown in Figure 6–5. The dummy variable (V_A) is inserted to make the calculations easier, and a is the op amp open loop gain.

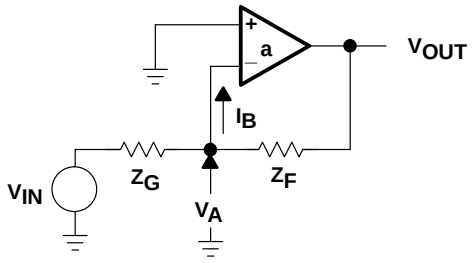

Figure 6–5. Inverting Op Amp

The transfer equation is given in Equation 6–16:

$$V_{OUT} = -aV_A \tag{6–16}$$

The node voltage (Equation 6–17) is obtained with the aid of superposition and the voltage divider rule. Equation 6–18 is obtained by combining Equations 6–16 and 6–17.

$$V_A = \frac{V_{IN} Z_F}{Z_G + Z_F} + \frac{V_{OUT} Z_G}{Z_G + Z_F} \quad \text{for } I_B = 0 \tag{6–17}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{-aZ_F}{Z_G + Z_F}}{1 + \dfrac{aZ_G}{Z_G + Z_F}} \tag{6–18}$$

Equation 6–16 is the transfer function of the inverting op amp. By virtue of the comparison between Equations 6–18 and 6–14, we get Equation 6–15 again, which is also the loop gain equation for the inverting op amp circuit. The comparison also shows that the open loop gain (A) is different from the op amp open loop gain (a) for the noninverting circuit.

The inverting op amp with the feedback loop broken is shown in Figure 6–6, and this circuit is used to calculate the loop-gain given in Equation 6–19.

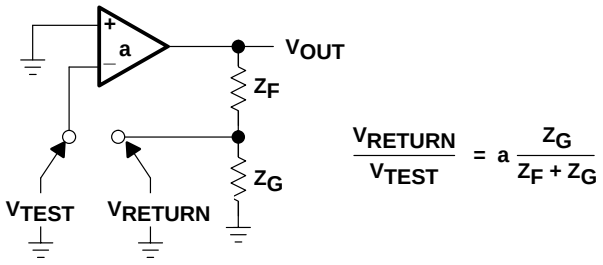

Figure 6–6. Inverting Op Amp: Feedback Loop Broken for Loop Gain Calculation

$$\frac{V_{RETURN}}{V_{TEST}} = \frac{aZ_G}{Z_G + Z_F} = A\beta \tag{6–19}$$

Several things must be mentioned at this point in the analysis. First, the transfer functions for the noninverting and inverting Equations, 6–13 and 6–18, are different. For a common set of Z_G and Z_F values, the magnitude and polarity of the gains are different. Second, the loop gain of both circuits, as given by Equations 6–15 and 6–19, is identical. Thus, the stability performance of both circuits is identical although their transfer equations are different. This makes the important point that *stability is not dependent on the circuit inputs*. Third, the A gain block shown in Figure 6–1 is different for each op amp circuit. By comparison of Equations 6–5, 6–11, and 6–18 we see that $A_{NON-INV} = a$ and $A_{INV} = aZ_F \div (Z_G + Z_F)$.

6.5 Differential Op Amps

The differential amplifier circuit is shown in Figure 6–7. The dummy variable, V_E, is inserted to make the calculations easier, and a is the open loop gain.

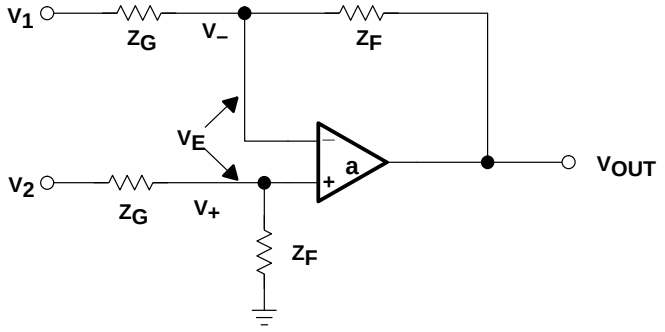

Figure 6–7. Differential Amplifier Circuit

Equation 6–20 is the circuit transfer equation.

$$V_{OUT} = a\,V_E = V_+ - V_- \tag{6–20}$$

The positive input voltage, V_+, is written in Equation 6–21 with the aid of superposition and the voltage divider rule.

$$V_+ = V_2 \frac{Z_F}{Z_F + Z_G} \tag{6–21}$$

The negative input voltage, V_-, is written in Equation 6–22 with the aid of superposition and the voltage divider rule.

$$V_- = V_1 \frac{Z_F}{Z_F + Z_G} - V_{OUT} \frac{Z_G}{Z_F + Z_G} \tag{6–22}$$

Combining Equations 6–20, 6–21, and 6–22 yields Equation 6–23.

$$V_{OUT} = a\left[\frac{V_2 Z_F}{Z_F + Z_G} - \frac{V_1 Z_F}{Z_F + Z_G} - \frac{V_{OUT} Z_G}{Z_F + Z_G}\right] \tag{6–23}$$

After algebraic manipulation, Equation 6–23 reduces to Equation 6–24.

$$\frac{V_{OUT}}{V_2 - V_1} = \frac{\frac{aZ_F}{Z_F + Z_G}}{1 + \frac{aZ_G}{Z_F + Z_G}} \tag{6–24}$$

The comparison method reveals that the loop gain as shown in Equation 6–25 is identical to that shown in Equations 6–13 and 6–19.

$$A\beta = \frac{aZ_G}{Z_G + Z_F} \tag{6–25}$$

Again, the loop gain, which determines stability, is only a function of the closed loop, and independent of the inputs.

Chapter 7

Voltage-Feedback Op Amp Compensation

Ron Mancini

7.1 Introduction

Voltage-feedback amplifiers (VFA) have been with us for about 60 years, and they have been problems for circuit designers since the first day. You see, the feedback that makes them versatile and accurate also has a tendency to make them unstable. The operational amplifier (op amp) circuit configuration uses a high-gain amplifier whose parameters are determined by external feedback components. The amplifier gain is so high that without these external feedback components, the slightest input signal would saturate the amplifier output. The op amp is in common usage, so this configuration is examined in detail, but the results are applicable to many other voltage-feedback circuits. Current-feedback amplifiers (CFA) are similar to VFAs, but the differences are important enough to warrant CFAs being handled separately.

Stability as used in electronic circuit terminology is often defined as achieving a nonoscillatory state. This is a poor, inaccurate definition of the word. Stability is a relative term, and this situation makes people uneasy because relative judgments are exhaustive. It is easy to draw the line between a circuit that oscillates and one that does not oscillate, so we can understand why some people believe that oscillation is a natural boundary between stability and instability.

Feedback circuits exhibit poor phase response, overshoot, and ringing long before oscillation occurs, and these effects are considered undesirable by circuit designers. This chapter is not concerned with oscillators; thus, relative stability is defined in terms of performance. By definition, when designers decide what tradeoffs are acceptable, they determine what the relative stability of the circuit is. A relative stability measurement is the damping ratio (ζ) and the damping ratio is discussed in detail in Reference 1. The damping ratio is related to phase margin, hence phase margin is another measure of relative stability. The most stable circuits have the longest response times, lowest bandwidth, highest accuracy, and least overshoot. The least stable circuits have the fastest response times, highest bandwidth, lowest accuracy, and some overshoot.

Op Amps left in their native state oscillate without some form of compensation. The first IC op amps were very hard to stabilize, but there were a lot of good analog designers

around in the ’60s, so we used them. Internally compensated op amps were introduced in the late ’60s in an attempt to make op amps easy for everyone to use. Unfortunately, internally compensated op amps sacrifice a lot of bandwidth and still oscillate under some conditions, so an understanding of compensation is required to apply op amps.

Internal compensation provides a worst-case trade-off between stability and performance. Uncompensated op amps require more attention, but they can do more work. Both are covered here.

Compensation is a process of applying a judicious patch in the form of an RC network to make up for a less than perfect op amp or circuit. There are many different problems that can introduce instability, thus there are many different compensation schemes.

7.2 Internal Compensation

Op amps are internally compensated to save external components and to enable their use by less knowledgeable people. It takes some measure of analog knowledge to compensate an analog circuit. Internally compensated op amps normally are stable when they are used in accordance with the applications instructions. Internally compensated op amps are not unconditionally stable. They are multiple pole systems, but they are internally compensated such that they appear as a single pole system over much of the frequency range. Internal compensation severely decreases the possible closed-loop bandwidth of the op amp.

Internal compensation is accomplished in several ways, but the most common method is to connect a capacitor across the collector-base junction of a voltage gain transistor (see Figure 7–1). The Miller effect multiplies the capacitor value by an amount approximately equal to the stage gain, thus the Miller effect uses small value capacitors for compensation.

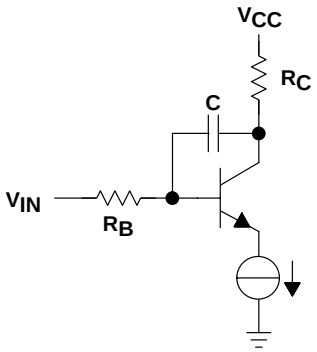

Figure 7–1. Miller Effect Compensation

Figure 7–2 shows the gain/phase diagram for an older op amp (TL03X). When the gain crosses the 0-dB axis (gain equal to one) the phase shift is approximately 108°, thus the op amp must be modeled as a second-order system because the phase shift is more than 90°.

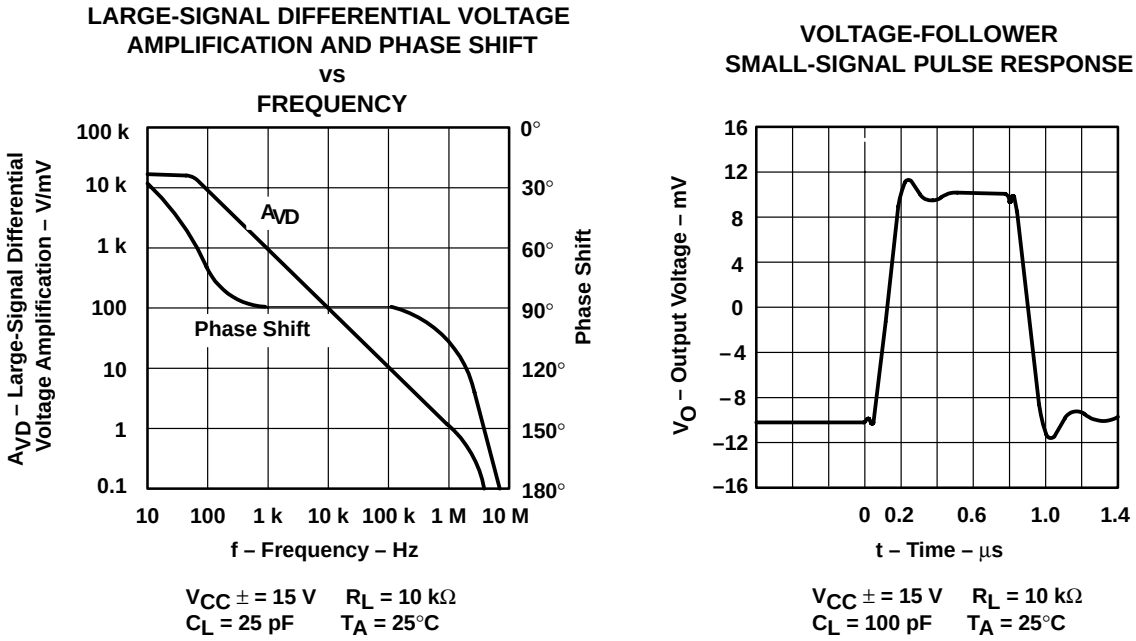

Figure 7–2. TL03X Frequency and Time Response Plots

This yields a phase margin of $\phi = 180° - 108° = 72°$, thus the circuit should be very stable. Referring to Figure 7–3, the damping ratio is one and the expected overshoot is zero. Figure 7–2 shows approximately 10% overshoot, which is unexpected, but inspecting Figure 7–2 further reveals that the loading capacitance for the two plots is different. The pulse response is loaded with 100 pF rather than 25 pF shown for the gain/phase plot, and this extra loading capacitance accounts for the loss of phase margin.

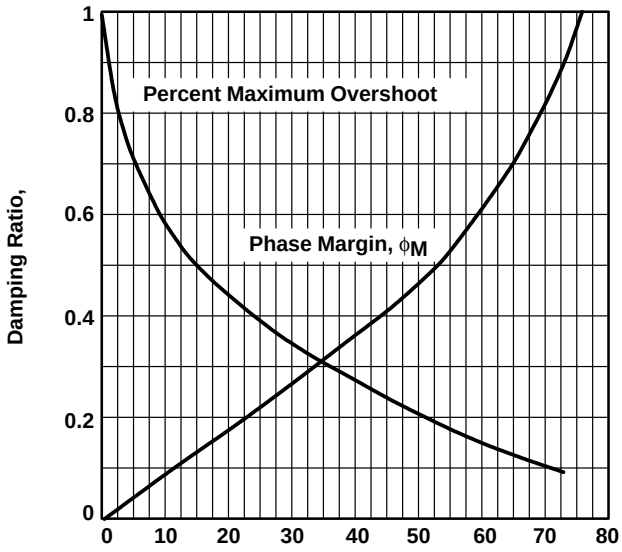

Figure 7–3. Phase Margin and Percent Overshoot Versus Damping Ratio

Why does the loading capacitance make the op amp unstable? Look closely at the gain/phase response between 1 MHz and 9 MHz, and observe that the gain curve changes slope drastically while the rate of phase change approaches 120°/decade. The radical gain/phase slope change proves that several poles are located in this area. The loading capacitance works with the op amp output impedance to form another pole, and the new pole reacts with the internal op amp poles. As the loading capacitor value is increased, its pole migrates down in frequency, causing more phase shift at the 0-dB crossover frequency. The proof of this is given in the TL03X data sheet where plots of ringing and oscillation versus loading capacitance are shown.

Figure 7–4 shows similar plots for the TL07X, which is the newer family of op amps. Notice that the phase shift is approximately 100° when the gain crosses the 0-dB axis. This yields a phase margin of 80°, which is close to unconditionally stable. The slope of the phase curve changes to 180°/decade about one decade from the 0-dB crossover point. The radical slope change causes suspicion about the 90° phase margin, furthermore the gain curve must be changing radically when the phase is changing radically. The gain/phase plot may not be totally false, but it sure is overly optimistic.

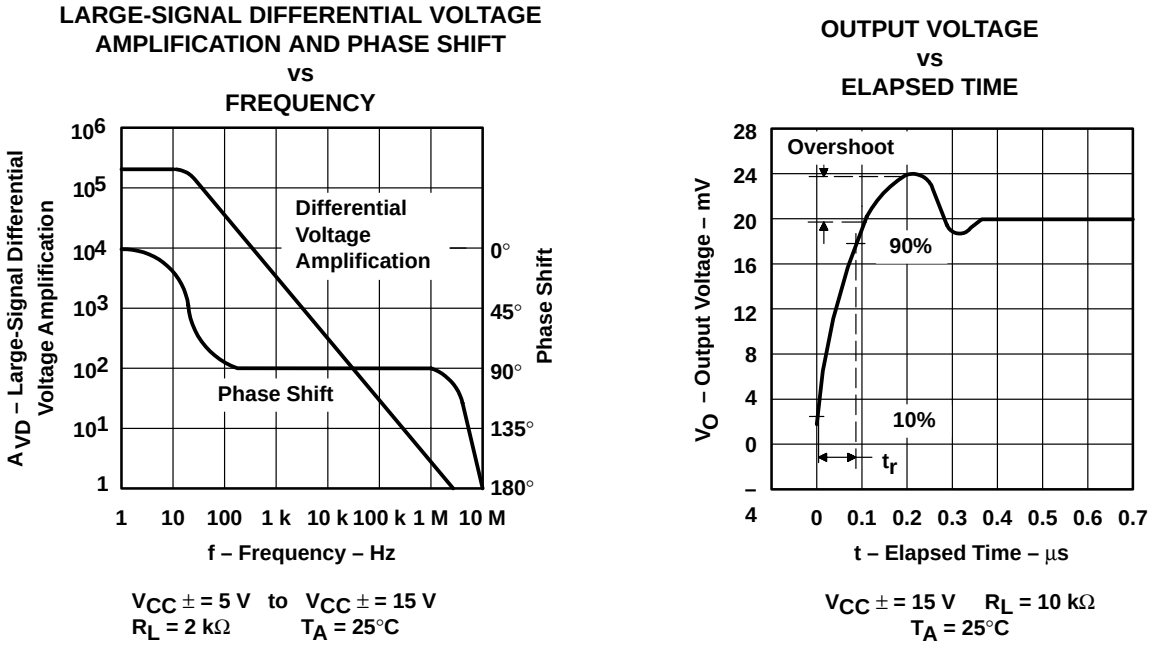

Figure 7–4. TL07X Frequency and Time Response Plots

The TL07X pulse response plot shows approximately 20% overshoot. There is no loading capacitance indicated on the plot to account for a seemingly unconditionally stable op amp exhibiting this large an overshoot. Something is wrong here: the analysis is wrong, the plots are wrong, or the parameters are wrong. Figure 7–5 shows the plots for the TL08X family of op amps, which are sisters to the TL07X family. The gain/phase curve and pulse response is virtually identical, but the pulse response lists a 100 pF loading capacitor. This little exercise illustrates three valuable points: first, if the data seems wrong it probably is wrong, second, even the factory people make mistakes, and third, the loading capacitor makes op amps ring, overshoot, or oscillate.

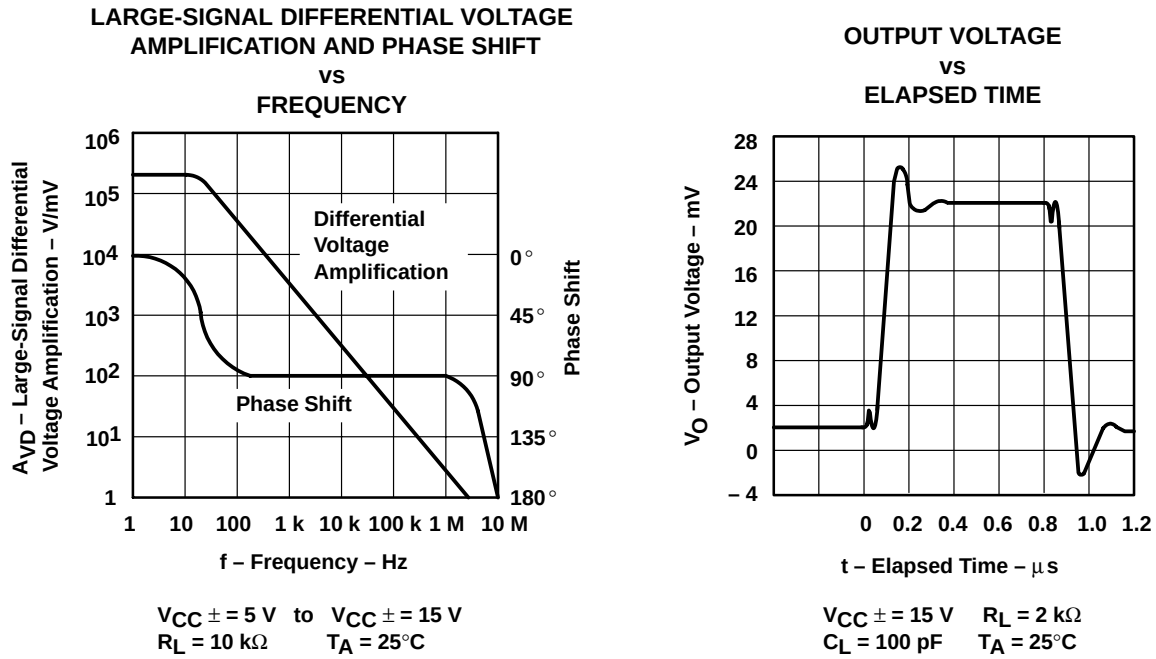

Figure 7–5. TL08X Frequency and Time Response Plots

The frequency and time-response plots for the TLV277X family of op amps is shown in Figures 7–6 and 7–7. First, notice that the information is more sophisticated because the phase response is given in degrees of phase margin; second, both gain/phase plots are done with substantial loading capacitors (600 pF), so they have some practical value; and third, the phase margin is a function of power supply voltage.

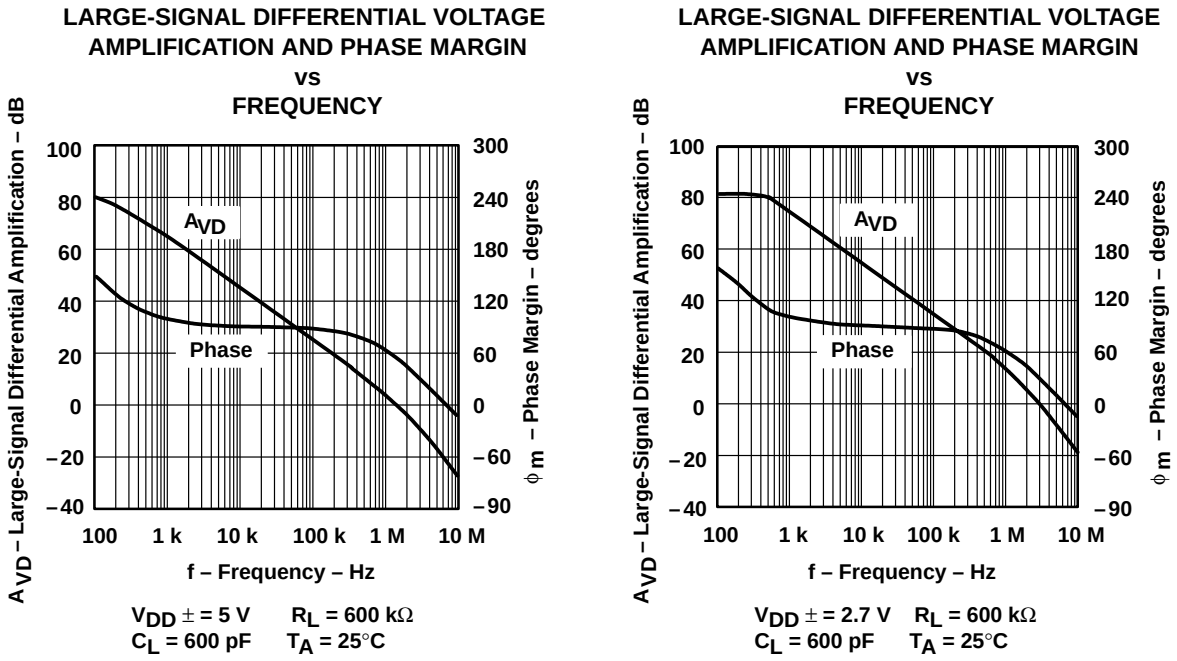

Figure 7–6. TLV277X Frequency Response Plots

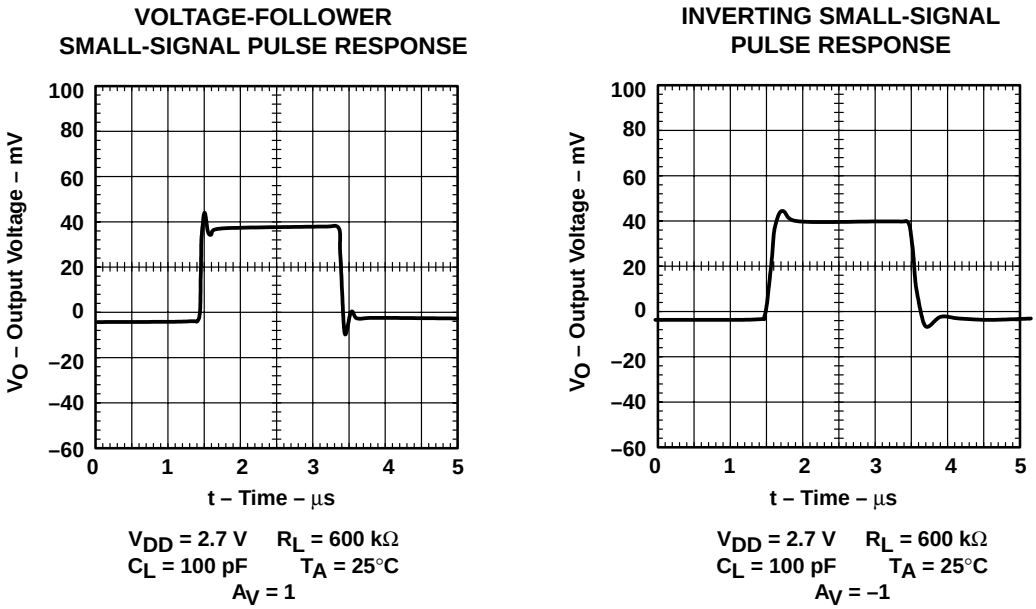

Figure 7–7. TLV227X Time Response Plots

At V_{CC} = 5 V, the phase margin at the 0-dB crossover point is 60°, while it is 30° at V_{CC} = 2.7 V. This translates into an expected overshoot of 18% at V_{CC} = 5 V, and 28% at V_{CC} = 2.7 V. Unfortunately the time response plots are done with 100-pF loading capacitance, hence we can not check our figures very well. The V_{CC} = 2.7 V overshoot is approximately 2%, and it is almost impossible to figure out what the overshoot would have been with a 600 pF loading capacitor. The small-signal pulse response is done with mV-signals, and that is a more realistic measurement than using the full signal swing.

Internally compensated op amps are very desirable because they are easy to use, and they do not require external compensation components. Their drawback is that the bandwidth is limited by the internal compensation scheme. The op amp open-loop gain eventually (when it shows up in the loop gain) determines the error in an op amp circuit. In a noninverting buffer configuration, the TL277X is limited to 1% error at 50 kHz (V_{CC} = 2.7 V) because the op amp gain is 40 dB at that point. Circuit designers can play tricks such as bypassing the op amp with a capacitor to emphasize the high-frequency gain, but the error is still 1%. Keep Equation 7–1 in mind because it defines the error. If the TLV277X were not internally compensated, it could be externally compensated for a lower error at 50 kHz because the gain would be much higher.

$$E = \frac{V_{IN}}{1 + A\beta} \tag{7–1}$$

7.3 External Compensation, Stability, and Performance

Nobody compensates an op amp just because it is there; they have a reason to compensate the op amp, and that reason is usually stability. They want the op amp to perform a function in a circuit where it is potentially unstable. Internally and noninternally compensated op amps are compensated externally because certain circuit configurations do cause oscillations. Several potentially unstable circuit configurations are analyzed in this section, and the reader can extend the external compensation techniques as required.

Other reasons for externally compensating op amps are noise reduction, flat amplitude response, and obtaining the highest bandwidth possible from an op amp. An op amp generates noise, and noise is generated by the system. The noise contains many frequency components, and when a high-pass filter is incorporated in the signal path, it reduces high frequency noise. Compensation can be employed to roll off the op amp's high frequency, closed-loop response, thus causing the op amp to act as a noise filter. Internally compensated op amps are modeled with a second order equation, and this means that the output voltage can overshoot in response to a step input. When this overshoot (or peaking) is undesirable, external compensation can increase the phase margin to 90° where there is no peaking. An uncompensated op amp has the highest bandwidth possible. External compensation is required to stabilize uncompensated op amps, but the compensation can be tailored to the specific circuit, thus yielding the highest possible bandwidth consistent with the pulse response requirements.

7.4 Dominant-Pole Compensation

We saw that capacitive loading caused potential instabilities, thus an op amp loaded with an output capacitor is a circuit configuration that must be analyzed. This circuit is called dominant pole compensation because if the pole formed by the op amp output impedance and the loading capacitor is located close to the zero frequency axis, it becomes dominant. The op amp circuit is shown in Figure 7–8, and the open loop circuit used to calculate the loop gain (Aβ) is shown in Figure 7–9.

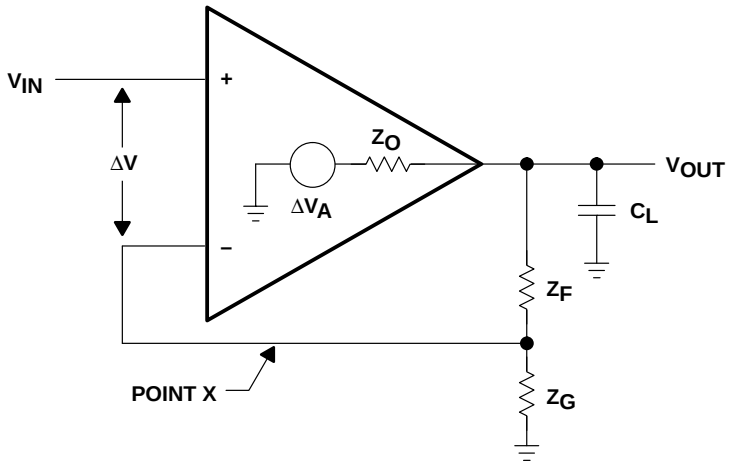

Figure 7–8. Capacitively-Loaded Op Amp

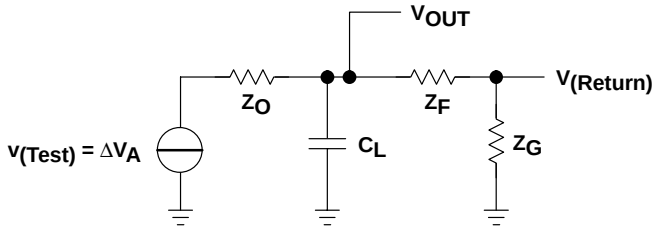

Figure 7–9. Capacitively-Loaded Op Amp With Loop Broken for Loop Gain (Aβ) Calculation

The analysis starts by looking into the capacitor and taking the Thevenin equivalent circuit.

$$V_{TH} = \frac{\Delta Va}{Z_O C_L s + 1} \tag{7–2}$$

$$Z_{TH} = \frac{Z_O}{Z_O C_L s + 1} \tag{7–3}$$

Then the output equation is written.

$$V_{RETURN} = \frac{V_{TH} Z_G}{Z_G + Z_F + Z_{TH}} = \frac{\Delta Va}{Z_O C_L s + 1} \left(\frac{Z_G}{Z_F + Z_G + \frac{Z_O}{Z_O C_L s + 1}} \right) \quad (7\text{–}4)$$

Rearranging terms yields Equation 7–5.

$$\frac{V_{RETURN}}{V_{TEST}} = A\beta = \frac{\frac{aZ_G}{Z_F + Z_G + Z_O}}{\frac{(Z_F + Z_G) Z_O C_L s}{Z_F + Z_G + Z_O} + 1} \quad (7\text{–}5)$$

When the assumption is made that $(Z_F + Z_G) >> Z_O$, Equation 7–5 reduces to Equation 7–6.

$$A\beta = \frac{aZ_G}{Z_F + Z_G} \left(\frac{1}{Z_O C_L s + 1} \right) \quad (7\text{–}6)$$

Equation 7–7 models the op amp as a second-order system. Hence, substituting the second-order model for *a* in Equation 7–6 yields Equation 7–8, which is the stability equation for the dominant-pole compensation circuit.

$$a = \frac{K}{(s + \tau_1)(s + \tau_2)} \quad (7\text{–}7)$$

$$A\beta = \frac{K}{(s + \tau_1)(s + \tau_2)} \frac{Z_G}{Z_F + Z_G} \frac{1}{Z_O C_L s + 1} \quad (7\text{–}8)$$

Several conclusions can be drawn from Equation 7–8 depending on the location of the poles. If the Bode plot of Equation 7–7, the op amp transfer function, looks like that shown in Figure 7–10, it only has 25° phase margin, and there is approximately 48% overshoot. When the pole introduced by Z_O and C_L moves towards the zero frequency axis it comes close to the τ_2 pole, and it adds phase shift to the system. Increased phase shift increases peaking and decreases stability. In the real world, many loads, especially cables, are capacitive, and an op amp like the one pictured in Figure 7–10 would ring while driving a capacitive load. The load capacitance causes peaking and instability in internally compensated op amps when the op amps do not have enough phase margin to allow for the phase shift introduced by the load.

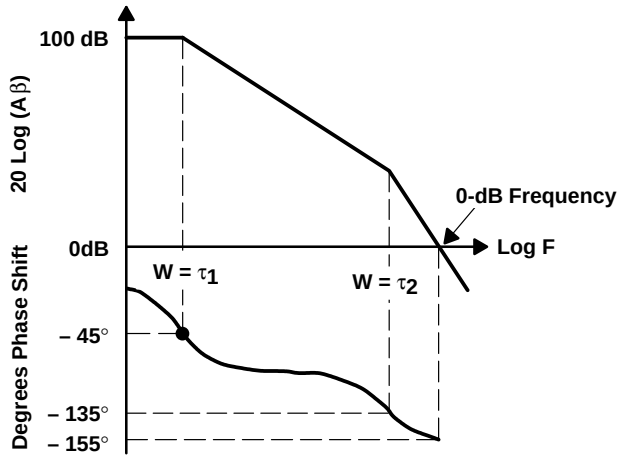

Figure 7–10. Possible Bode Plot of the Op Amp Described in Equation 7–7

Prior to compensation, the Bode plot of an uncompensated op amp looks like that shown in Figure 7–11. Notice that the break points are located close together thus accumulating about 180° of phase shift before the 0 dB crossover point; the op amp is not usable and probably unstable. Dominant pole compensation is often used to stabilize these op amps. If a dominant pole, in this case ω_D, is properly placed it rolls off the gain so that τ_1 introduces 45° phase at the 0-dB crossover point. After the dominant pole is introduced the op amp is stable with 45° phase margin, but the op amp gain is drastically reduced for frequencies higher than ω_D. This procedure works well for internally compensated op amps, but is seldom used for externally compensated op amps because inexpensive discrete capacitors are readily available.

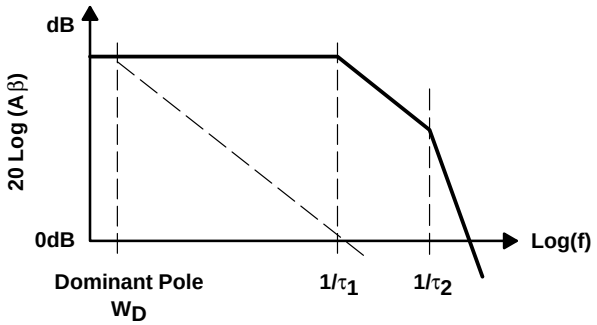

Figure 7–11. Dominant-Pole Compensation Plot

Assuming that $Z_O << Z_F$, the closed-loop transfer function is easy to calculate because C_L is enclosed in the feedback loop. The ideal closed-loop transfer equation is the same as Equation 6–11 for the noninverting op amp, and is repeated below as Equation 7–9.

$$\frac{V_{OUT}}{V_{IN}} = \frac{a}{1 + \frac{aZ_G}{Z_G + Z_F}} \tag{7–9}$$

When a $\Rightarrow \infty$ Equation 7–9 reduces to Equation 7–10.

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_F + Z_G}{Z_G} \tag{7–10}$$

As long as the op amp has enough compliance and current to drive the capacitive load, and Z_O is small, the circuit functions as though the capacitor was not there. When the capacitor becomes large enough, its pole interacts with the op amp pole causing instability. When the capacitor is huge, it completely kills the op amp's bandwidth, thus lowering the noise while retaining a large low-frequency gain.

7.5 Gain Compensation

When the closed-loop gain of an op amp circuit is related to the loop gain, as it is in voltage-feedback op amps, the closed-loop gain can be used to stabilize the circuit. This type of compensation can not be used in current-feedback op amps because the mathematical relationship between the loop gain and ideal closed-loop gain does not exist. The loop gain equation is repeated as Equation 7–11. Notice that the closed-loop gain parameters Z_G and Z_F are contained in Equation 7–11, hence the stability can be controlled by manipulating the closed-loop gain parameters.

$$A\beta = \frac{aZ_G}{Z_G + Z_F} \tag{7–11}$$

The original loop gain curve for a closed-loop gain of one is shown in Figure 7–12, and it is or comes very close to being unstable. If the closed-loop noninverting gain is changed to 9, then K changes from K/2 to K/10. The loop gain intercept on the Bode plot (Figure 7–12) moves down 14 dB, and the circuit is stabilized.

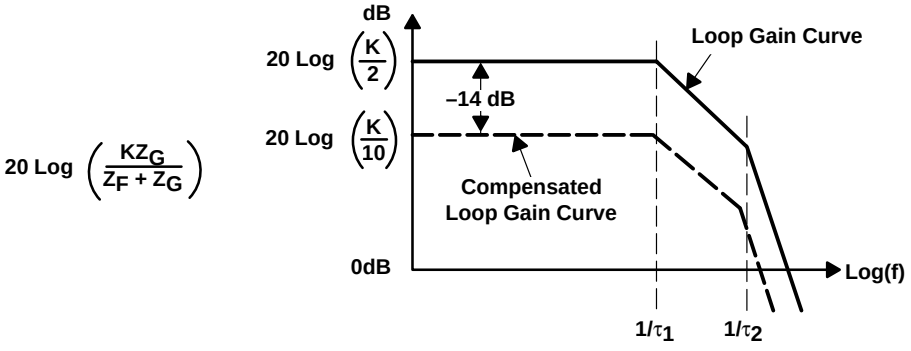

Figure 7–12. Gain Compensation

Gain compensation works for inverting or noninverting op amp circuits because the loop gain equation contains the closed-loop gain parameters in both cases. When the closed-loop gain is increased, the accuracy and the bandwidth decrease. As long as the application can stand the higher gain, gain compensation is the best type of compensation to use. Uncompensated versions of normally internally compensated op amps are offered for sale as stable op amps with minimum gain restrictions. As long as gain in the circuit you design exceeds the gain specified on the data sheet, this is economical and a safe mode of operation.

7.6 Lead Compensation

Sometimes lead compensation is forced on the circuit designer because of the parasitic capacitance associated with packaging and wiring op amps. Figure 7–13 shows the circuit for lead compensation; notice the capacitor in parallel with R_F. That capacitor is often made by parasitic wiring and the ground plane, and high frequency circuit designers go to great lengths to minimize or eliminate it. What is good in one sense is bad in another, because adding the parallel capacitor is a good way to stabilize the op amp and reduce noise. Let us analyze the stability first, and then we will analyze the closed-loop performance.

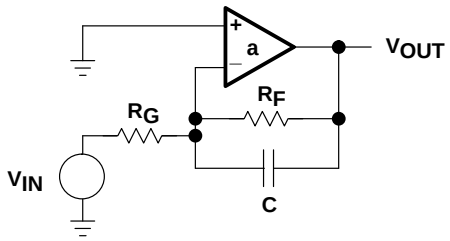

Figure 7–13. Lead-Compensation Circuit

The loop equation for the lead-compensation circuit is given by Equation 7–12.

$$A\beta = \left(\frac{R_G}{R_G + R_F}\right)\left(\frac{R_F Cs + 1}{R_G \parallel R_F Cs + 1}\right)\left[\frac{K}{(s + \tau_1)(s + \tau_2)}\right] \qquad (7\text{–}12)$$

The compensation capacitor introduces a pole and zero into the loop equation. The zero always occurs before the pole because $R_F > R_F || R_G$. When the zero is properly placed it cancels out the τ_2 pole along with its associated phase shift. The original transfer function is shown in Figure 7–14 drawn in solid lines. When the $R_F C$ zero is placed at $\omega = 1/\tau_2$, it cancels out the τ_2 pole causing the bode plot to continue on a slope of –20 dB/decade. When the frequency gets to $\omega = 1/(R_F||RG)C$, this pole changes the slope to –40 dB/decade. Properly placed, the capacitor aids stability, but what does it do to the closed-loop

transfer function? The equation for the inverting op amp closed-loop gain is repeated below.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{-aZ_F}{Z_G + Z_F}}{1 + \frac{aZ_G}{Z_G + Z_F}} \tag{7–13}$$

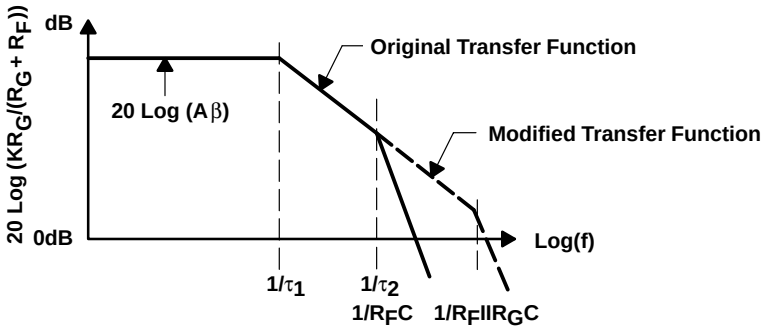

Figure 7–14. Lead-Compensation Bode Plot

When *a* approaches infinity, Equation 7–13 reduces to Equation 7–14.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_F}{Z_{IN}} \tag{7–14}$$

Substituting R_F || C for Z_F and R_G for Z_G in Equation 7–14 yields Equation 7–15, which is the ideal closed-loop gain equation for the lead compensation circuit.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_G}\left(\frac{1}{R_F Cs + 1}\right) \tag{7–15}$$

The forward gain for the inverting amplifier is given by Equation 7–16. Compare Equation 7–13 with Equation 6–5 to determine A.

$$A = \frac{aZ_F}{Z_G + A_F} = \left(\frac{aR_F}{R_G + R_F}\right)\left(\frac{1}{R_F \parallel R_G Cs + 1}\right) \tag{7–16}$$

The op amp gain (a), the forward gain (A), and the ideal closed-loop gain are plotted in Figure 7–15. The op amp gain is plotted for reference only. The forward gain for the inverting op amp is not the op amp gain. Notice that the forward gain is reduced by the factor $R_F/(R_G + R_F)$, and it contains a high frequency pole. The ideal closed-loop gain follows the ideal curve until the $1/R_FC$ breakpoint (same location as $1/\tau_2$ breakpoint), and then it

slopes down at –20 dB/decade. Lead compensation sacrifices the bandwidth between the $1/R_FC$ breakpoint and the forward gain curve. The location of the $1/R_FC$ pole determines the bandwidth sacrifice, and it can be much greater than shown here. The pole caused by R_F, R_G, and C does not appear until the op amp's gain has crossed the 0-dB axis, thus it does not affect the ideal closed-loop transfer function.

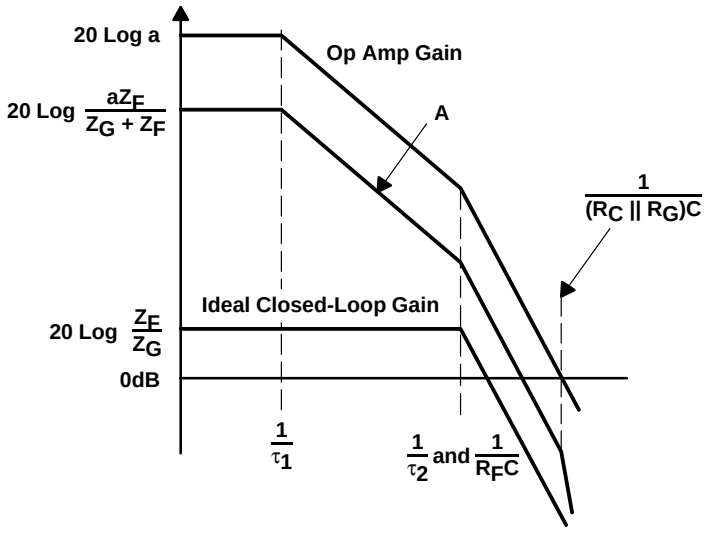

Figure 7–15. Inverting Op Amp With Lead Compensation

The forward gain for the noninverting op amp is *a*; compare Equation 6–11 to Equation 6–5. The ideal closed-loop gain is given by Equation 7–17.

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_F + Z_G}{Z_G} = \left(\frac{R_F + R_G}{R_G}\right)\left(\frac{R_F \| R_G Cs + 1}{R_F Cs + 1}\right) \qquad (7\text{–}17)$$

The plot of the noninverting op amp with lead compensation is shown in Figure 7–16. There is only one plot for both the op amp gain (a) and the forward gain (A), because they are identical in the noninverting circuit configuration. The ideal starts out as a flat line, but it slopes down because its closed-loop gain contains a pole and a zero. The pole always occurs closer to the low frequency axis because $R_F > R_F||R_G$. The zero flattens the ideal closed-loop gain curve, but it never does any good because it cannot fall on the pole. The pole causes a loss in the closed-loop bandwidth by the amount separating the closed-loop and forward gain curves.

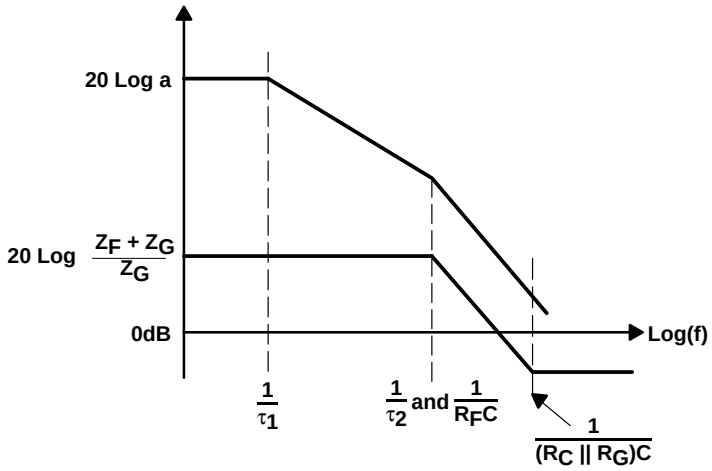

Figure 7–16. Noninverting Op Amp With Lead Compensation

Although the forward gain is different in the inverting and noninverting circuits, the closed-loop transfer functions take very similar shapes. This becomes truer as the closed-loop gain increases because the noninverting forward gain approaches the op amp gain. This relationship cannot be relied on in every situation, and each circuit must be checked to determine the closed-loop effects of the compensation scheme.

7.7 Compensated Attenuator Applied to Op Amp

Stray capacitance on op amp inputs is a problem that circuit designers are always trying to get away from because it decreases stability and causes peaking. The circuit shown in Figure 7–17 has some stray capacitance (C_G,) connected from the inverting input to ground. Equation 7–18 is the loop gain equation for the circuit with input capacitance.

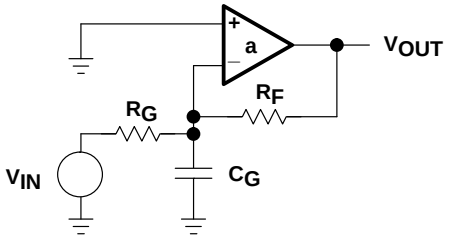

Figure 7–17. Op Amp With Stray Capacitance on the Inverting Input

$$A\beta = \left(\frac{R_G}{R_G + R_F}\right)\left(\frac{1}{R_G \parallel R_F Cs + 1}\right)\left[\frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)}\right] \quad (7\text{–}18)$$

Op amps having high input and feedback resistors are subject to instability caused by stray capacitance on the inverting input. Referring to Equation 7–18, when the

$1/(R_F||R_GC_G)$ pole moves close to τ_2 the stage is set for instability. Reasonable component values for a CMOS op amp are $R_F = 1\ M\Omega$, $R_G = 1\ M\Omega$, and $C_G = 10$ pF. The resulting pole occurs at 318 kHz, and this frequency is lower than the breakpoint of τ_2 for many op amps. There is 90° of phase shift resulting from τ_1, the $1/(R_F||R_GC)$ pole adds 45° phase shift at 318 kHz, and τ_2 starts to add another 45° phase shift at about 600 kHz. This circuit is unstable because of the stray input capacitance. The circuit is compensated by adding a feedback capacitor as shown in Figure 7–18.

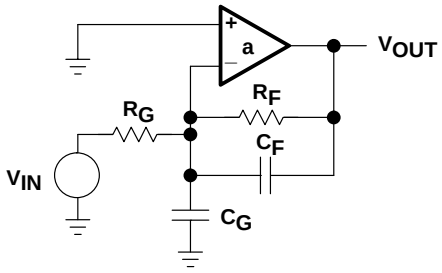

Figure 7–18. Compensated Attenuator Circuit

The loop gain with C_F added is given by Equation 7–19.

$$A\beta = \left[\frac{\frac{R_G}{R_GC_Gs+1}}{\frac{R_G}{R_GC_Gs+1}+\frac{R_F}{R_FC_Fs+1}}\right]\left[\frac{K}{(\tau_1 s+1)(\tau_2 s+1)}\right] \qquad (7\text{–}19)$$

If $R_GC_G = R_FC_F$ Equation 7–19 reduces to Equation 7–20.

$$A\beta = \left(\frac{R_G}{R_G+R_F}\right)\left[\frac{K}{(\tau_1 s+1)(\tau_2 s+1)}\right] \qquad (7\text{–}20)$$

The compensated attenuator Bode plot is shown in Figure 7–19. Adding the correct $1/R_FC_F$ breakpoint cancels out the $1/R_GC_G$ breakpoint; the loop gain is independent of the capacitors. Now is the time to take advantage of the stray capacitance. C_F can be formed by running a wide copper strip from the output of the op amp over the ground plane under R_F; do not connect the other end of this copper strip. The circuit is tuned by removing some copper (a razor works well) until all peaking is eliminated. Then measure the copper, and have an identical trace put on the printed-circuit board.

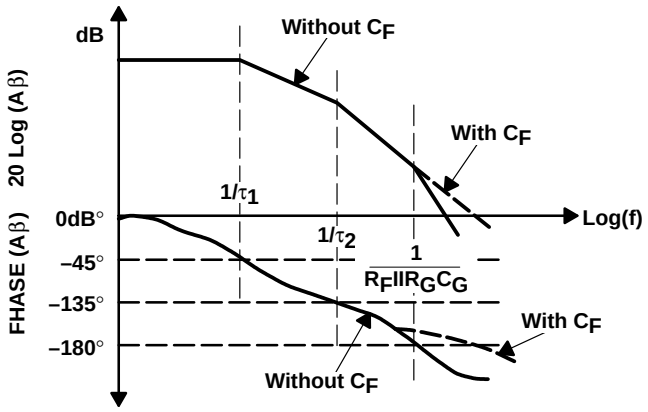

Figure 7–19. Compensated Attenuator Bode Plot

The inverting and noninverting closed-loop gain equations are a function of frequency. Equation 7–21 is the closed-loop gain equation for the inverting op amp. When $R_F C_F = R_G C_G$, Equation 7–21 reduces to Equation 7–22, which is independent of the breakpoint. This also happens to the noninverting op amp circuit. This is one of the few occasions when the compensation does not affect the closed-loop gain frequency response.

$$\frac{V_{OUT}}{V_{IN}} = - \frac{\frac{R_F}{R_F C_F s + 1}}{\frac{R_G}{R_G C_G s + 1}} \tag{7–21}$$

When $R_F C_F = R_G C_G$

$$\frac{V_{OUT}}{V_{IN}} = - \left(\frac{R_F}{R_G} \right) \tag{7–22}$$

7.8 Lead-Lag Compensation

Lead-lag compensation stabilizes the circuit without sacrificing the closed-loop gain performance. It is often used with uncompensated op amps. This type of compensation provides excellent high-frequency performance. The circuit schematic is shown in Figure 7–20, and the loop gain is given by Equation 7–23.

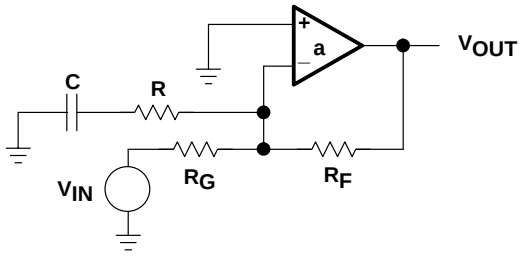

Figure 7–20. Lead-Lag Compensated Op Amp

$$A\beta = \frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)} \frac{R_G}{R_G + R_F} \frac{RCs + 1}{\frac{(RR_G + RR_F + R_G R_F)}{(R_G + R_F)} Cs + 1} \qquad (7\text{–}23)$$

Referring to Figure 7–21, a pole is introduced at $\omega = 1/RC$, and this pole reduces the gain 3 dB at the breakpoint. When the zero occurs prior to the first op amp pole it cancels out the phase shift caused by the $\omega = 1/RC$ pole. The phase shift is completely canceled before the second op amp pole occurs, and the circuit reacts as if the pole was never introduced. Nevertheless, $A\beta$ is reduced by 3 dB or more, so the loop gain crosses the 0-dB axis at a lower frequency. The beauty of lead lag compensation is that the closed-loop ideal gain is not affected as is shown below. The Thevenin equivalent of the input circuit is calculated in Equation 7–24, the circuit gain in terms of Thevenin equivalents is calculated in Equation 7–25, and the ideal closed-loop gain is calculated in Equation 7–26.

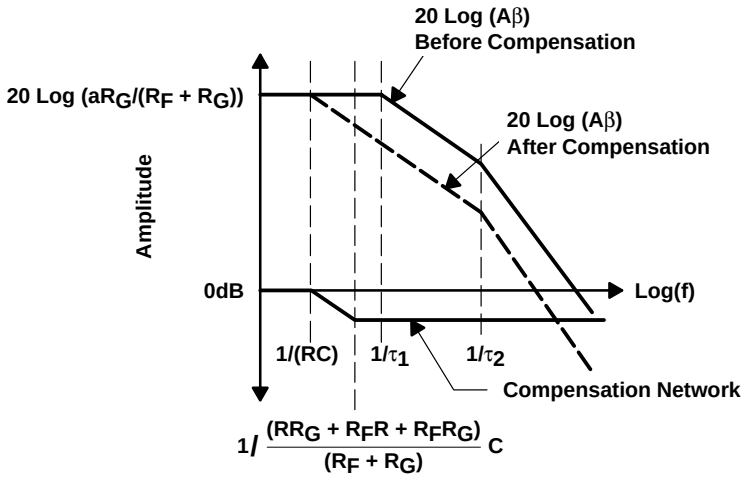

Figure 7–21. Bode Plot of Lead-Lag Compensated Op Amp

$$V_{TH} = V_{IN}\frac{R + \frac{1}{Cs}}{R + R_G + \frac{1}{Cs}} \qquad R_{TH} = \frac{R_G\left(R + \frac{1}{Cs}\right)}{R + R_G + \frac{1}{Cs}} \tag{7–24}$$

$$V_{OUT} = -V_{TH}\frac{R_F}{R_{TH}} \tag{7–25}$$

$$-\frac{V_{OUT}}{V_{IN}} = \frac{R + \frac{1}{Cs}}{R + R_G + \frac{1}{Cs}}\frac{R_F}{\frac{R_G\left(R+\frac{1}{Cs}\right)}{R+R_G+\frac{1}{Cs}}} = \frac{R_F}{R_G} \tag{7–26}$$

Equation 7–26 is intuitively obvious because the RC network is placed across a virtual ground. As long as the loop gain, Aβ, is large, the feedback will null out the closed-loop effect of RC, and the circuit will function as if it were not there. The closed-loop log plot of the lead-lag-compensated op amp is given in Figure 7–22. Notice that the pole and zero resulting from the compensation occur and are gone before the first amplifier poles come on the scene. This prevents interaction, but it is not required for stability.

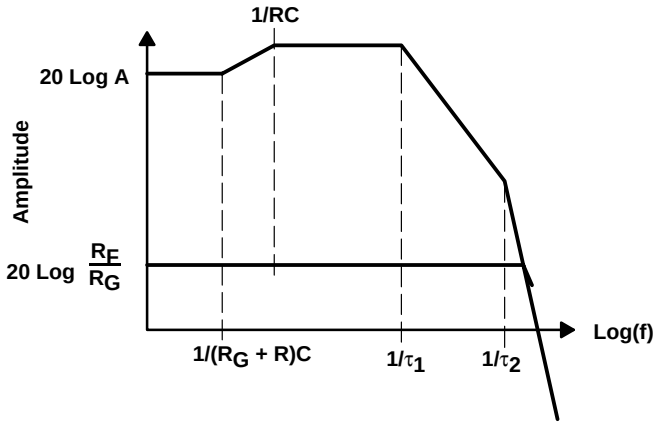

Figure 7–22. Closed-Loop Plot of Lead-Lag Compensated Op Amp

7.9 Comparison of Compensation Schemes

Internally compensated op amps can, and often do, oscillate under some circuit conditions. Internally compensated op amps need an external pole to get the oscillation or ringing started, and circuit stray capacitances often supply the phase shift required for instability. Loads, such as cables, often cause internally compensated op amps to ring severely.

Dominant pole compensation is often used in IC design because it is easy to implement. It rolls off the closed-loop gain early; thus, it is seldom used as an external form of compensation unless filtering is required. Load capacitance, depending on its pole location, usually causes the op amp to ring. Large load capacitance can stabilize the op amp because it acts as dominant pole compensation.

The simplest form of compensation is gain compensation. High closed-loop gains are reflected in lower loop gains, and in turn, lower loop gains increase stability. If an op amp circuit can be stabilized by increasing the closed-loop gain, do it.

Stray capacitance across the feedback resistor tends to stabilize the op amp because it is a form of lead compensation. This compensation scheme is useful for limiting the circuit bandwidth, but it decreases the closed-loop gain.

Stray capacitance on the inverting input works with the parallel combination of the feedback and gain setting resistors to form a pole in the Bode plot, and this pole decreases the circuit's stability. This effect is normally observed in high-impedance circuits built with CMOS op amps. Adding a feedback capacitor forms a compensated attenuator scheme that cancels out the input pole. The cancellation occurs when the input and feedback RC time constants are equal. Under the conditions of equal time constants, the op amp functions as though the stray input capacitance was not there. An excellent method of implementing a compensated attenuator is to build a stray feedback capacitor using the ground plane and a trace off the output node.

Lead-lag compensation stabilizes the op amp, and it yields the best closed-loop frequency performance. Contrary to some published opinions, no compensation scheme will increase the bandwidth beyond that of the op amp. Lead-lag compensation just gives the best bandwidth for the compensation.

7.10 Conclusions

The stability criteria often is not oscillation, rather it is circuit performance as exhibited by peaking and ringing.

The circuit bandwidth can often be increased by connecting an external capacitor in parallel with the op amp. Some op amps have hooks that enable a parallel capacitor to be connected in parallel with a portion of the input stages. This increases bandwidth because it shunts high frequencies past the low bandwidth g_m stages, but this method of compensation depends on the op amp type and manufacturer.

The compensation techniques given here are adequate for the majority of applications. When the new and challenging application presents itself, use the procedure outlined here to invent your own compensation technique.

Chapter 8

Current-Feedback Op Amp Analysis

Ron Mancini

8.1 Introduction

Current-feedback amplifiers (CFA) do not have the traditional differential amplifier input structure, thus they sacrifice the parameter matching inherent to that structure. The CFA circuit configuration prevents them from obtaining the precision of voltage-feedback amplifiers (VFA), but the circuit configuration that sacrifices precision results in increased bandwidth and slew rate. The higher bandwidth is relatively independent of closed-loop gain, so the constant gain-bandwidth restriction applied to VFAs is removed for CFAs. The slew rate of CFAs is much improved from their counterpart VFAs because their structure enables the output stage to supply slewing current until the output reaches its final value. In general, VFAs are used for precision and general purpose applications, while CFAs are restricted to high frequency applications above 100 MHz.

Although CFAs do not have the precision of their VFA counterparts, they are precise enough to be dc-coupled in video applications where dynamic range requirements are not severe. CFAs, unlike previous generation high-frequency amplifiers, have eliminated the ac coupling requirement; they are usually dc-coupled while they operate in the GHz range. CFAs have much faster slew rates than VFAs, so they have faster rise/fall times and less intermodulation distortion.

8.2 CFA Model

The CFA model is shown in Figure 8–1. The noninverting input of a CFA connects to the input of the input buffer, so it has very high impedance similar to that of a bipolar transistor noninverting VFA input. The inverting input connects to the input buffer's output, so the inverting input impedance is equivalent to a buffer's output impedance, which is very low. Z_B models the input buffer's output impedance, and it is usually less than 50 Ω. The input buffer gain, G_B, is as close to one as IC design methods can achieve, and it is small enough to neglect in the calculations.

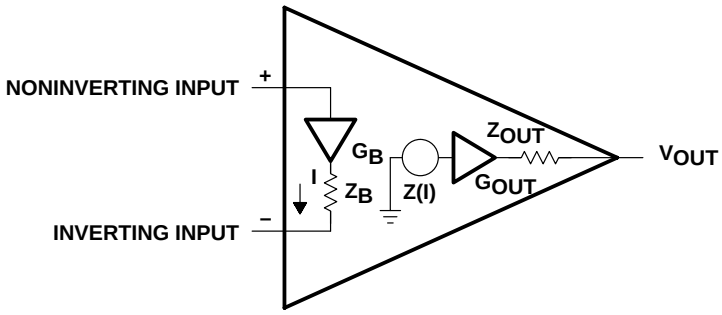

Figure 8–1. Current-Feedback Amplifier Model

The output buffer provides low output impedance for the amplifier. Again, the output buffer gain, G_{OUT}, is very close to one, so it is neglected in the analysis. The output impedance of the output buffer is ignored during the calculations. This parameter may influence the circuit performance when driving very low impedance or capacitive loads, but this is usually not the case. The input buffer's output impedance can't be ignored because affects stability at high frequencies.

The current-controlled current source, Z, is a transimpedance. The transimpedance in a CFA serves the same function as gain in a VFA; it is the parameter that makes the performance of the op amp dependent only on the passive parameter values. Usually the transimpedance is very high, in the MΩ range, so the CFA gains accuracy by closing a feedback loop in the same manner that the VFA does.

8.3 Development of the Stability Equation

The stability equation is developed with the aid of Figure 8–2. Remember, stability is independent of the input, and stability depends solely on the loop gain, Aβ. Breaking the loop at point *X*, inserting a test signal, V_{TI}, and calculating the return signal V_{TO} develops the stability equation.

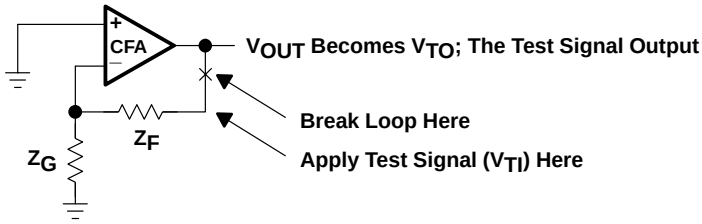

Figure 8–2. Stability Analysis Circuit

The circuit used for stability calculations is shown in Figure 8–3 where the model of Figure 8–1 is substituted for the CFA symbol. The input and output buffer gain, and output buffer

output impedance have been deleted from the circuit to simplify calculations. This approximation is valid for almost all applications.

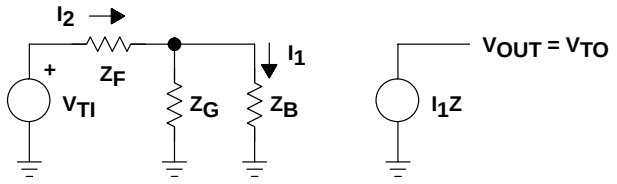

Figure 8–3. Stability Analysis Circuit

The transfer equation is given in Equation 8–1, and the Kirchoff"s law is used to write Equations 8–2 and 8–3.

$$V_{TO} = I_1 Z \tag{8–1}$$

$$V_{TI} = I_2\left(Z_F + Z_G \parallel Z_B\right) \tag{8–2}$$

$$I_2\left(Z_G \parallel Z_B\right) = I_1 Z_B \tag{8–3}$$

Equations 8–2 and 8–3 are combined to yield Equation 8–4.

$$V_{TI} = I_1\left(Z_F + Z_G \parallel Z_B\right)\left(1 + \frac{Z_B}{Z_G}\right) = I_1 Z_F\left(1 + \frac{Z_B}{Z_F \parallel Z_G}\right) \tag{8–4}$$

Dividing Equation 8–1 by Equation 8–4 yields Equation 8–5, and this is the open loop transfer equation. This equation is commonly known as the loop gain.

$$A\beta = \frac{V_{TO}}{V_{TI}} = \frac{Z}{\left(Z_F\left(1 + \frac{Z_B}{Z_F \parallel Z_G}\right)\right)} \tag{8–5}$$

8.4 The Noninverting CFA

The closed-loop gain equation for the noninverting CFA is developed with the aid of Figure 8–4, where external gain setting resistors have been added to the circuit. The buffers are shown in Figure 8–4, but because their gains equal one and they are included within the feedback loop, the buffer gain does not enter into the calculations.

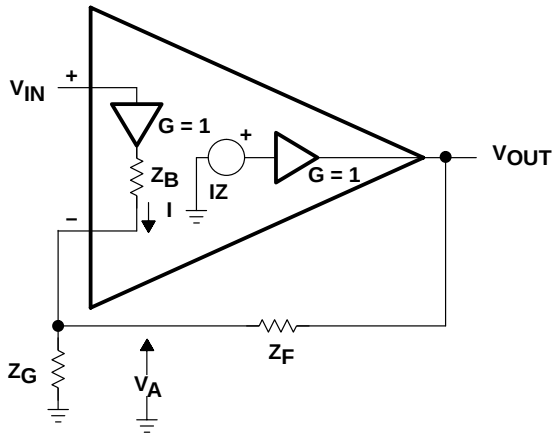

Figure 8–4. Noninverting CFA

Equation 8–6 is the transfer equation, Equation 8–7 is the current equation at the inverting node, and Equation 8–8 is the input loop equation. These equations are combined to yield the closed-loop gain equation, Equation 8–9.

$$V_{OUT} = IZ \tag{8–6}$$

$$I = \left(\frac{V_A}{Z_G}\right) - \left(\frac{V_{OUT} - V_A}{Z_F}\right) \tag{8–7}$$

$$V_A = V_{IN} - IZ_B \tag{8–8}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{Z\left(1 + \dfrac{Z_F}{Z_G}\right)}{Z_F\left(1 + \dfrac{Z_B}{Z_F \| Z_G}\right)}}{1 + \dfrac{Z}{Z_F\left(1 + \dfrac{Z_B}{Z_F \| Z_G}\right)}} \tag{8–9}$$

When the input buffer output impedance, Z_B, approaches zero, Equation 8–9 reduces to Equation 8–10.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{Z\left(1+\frac{Z_F}{Z_G}\right)}{Z_F}}{1+\frac{Z}{Z_F}} = \frac{1+\frac{Z_F}{Z_G}}{1+\frac{Z_F}{Z}} \qquad (8\text{–}10)$$

When the transimpedance, Z, is very high, the term Z_F/Z in Equation 8–10 approaches zero, and Equation 8–10 reduces to Equation 8–11; the ideal closed-loop gain equation for the CFA. The ideal closed-loop gain equations for the CFA and VFA are identical, and the degree to which they depart from ideal is dependent on the validity of the assumptions. The VFA has one assumption that the direct gain is very high, while the CFA has two assumptions, that the transimpedance is very high and that the input buffer output impedance is very low. As would be expected, two assumptions are much harder to meet than one, thus the CFA departs from the ideal more than the VFA does.

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{Z_F}{Z_G} \qquad (8\text{–}11)$$

8.5 The Inverting CFA

The inverting CFA configuration is seldom used because the inverting input impedance is very low ($Z_B||Z_F + Z_G$). When Z_G is made dominant by selecting it as a high resistance value it overrides the effect of Z_B. Z_F must also be selected as a high value to achieve at least unity gain, and high values for Z_F result in poor bandwidth performance, as we will see in the next section. If Z_G is selected as a low value the frequency sensitive Z_B causes the gain to increase as frequency increases. These limitations restrict inverting applications of the inverting CFA.

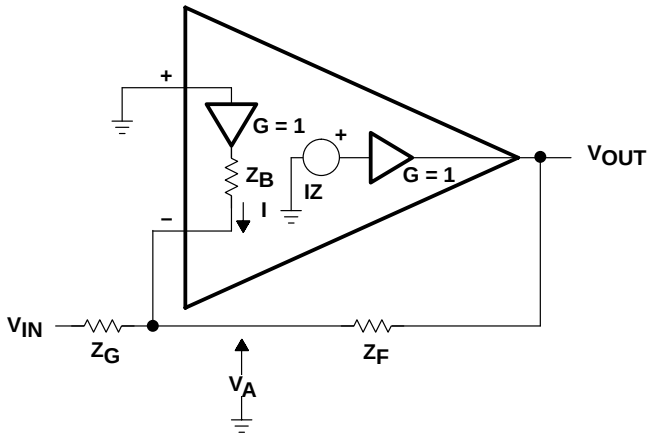

Figure 8–5. Inverting CFA

The current equation for the input node is written as Equation 8–12. Equation 8–13 defines the dummy variable, V_A, and Equation 8–14 is the transfer equation for the CFA. These equations are combined and simplified leading to Equation 8–15, which is the closed-loop gain equation for the inverting CFA.

$$I + \frac{V_{IN} - V_A}{Z_G} = \frac{V_A - V_{OUT}}{Z_F} \tag{8–12}$$

$$IZ_B = -V_A \tag{8–13}$$

$$IZ = V_{OUT} \tag{8–14}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{\dfrac{Z}{Z_G\left(1 + \dfrac{Z_B}{Z_F \| Z_G}\right)}}{1 + \dfrac{Z}{Z_F\left(1 + \dfrac{Z_B}{Z_F \| Z_G}\right)}} \tag{8–15}$$

When Z_B approaches zero, Equation 8–15 reduces to Equation 8–16.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{\dfrac{1}{Z_G}}{\dfrac{1}{Z} + \dfrac{1}{Z_F}} \tag{8–16}$$

When Z is very large, Equation 8–16 becomes Equation 8–17, which is the ideal closed-loop gain equation for the inverting CFA.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_F}{Z_G} \tag{8–17}$$

The ideal closed-loop gain equation for the inverting VFA and CFA op amps are identical. Both configurations have lower input impedance than the noninverting configuration has, but the VFA has one assumption while the CFA has two assumptions. Again, as was the case with the noninverting counterparts, the CFA is less ideal than the VFA because of the two assumptions. The zero Z_B assumption always breaks down in bipolar junction transistors as is shown later. The CFA is almost never used in the differential amplifier configuration because of the CFA's gross input impedance mismatch.

8.6 Stability Analysis

The stability equation is repeated as Equation 8–18.

$$A\beta = \frac{V_{TO}}{V_{TI}} = \frac{Z}{\left(Z_F\left(1 + \frac{Z_B}{Z_F \| Z_G}\right)\right)} \tag{8–18}$$

Comparing Equations 8–9 and 8–15 to Equation 8–18 reveals that the inverting and noninverting CFA op amps have identical stability equations. This is the expected result because stability of any feedback circuit is a function of the loop gain, and the input signals have no affect on stability. The two op amp parameters affecting stability are the transimpedance, Z, and the input buffer's output impedance, Z_B. The external components affecting stability are Z_G and Z_F. The designer controls the external impedance, although stray capacitance that is a part of the external impedance sometimes seems to be uncontrollable. Stray capacitance is the primary cause of ringing and overshoot in CFAs. Z and Z_B are CFA op amp parameters that can't be controlled by the circuit designer, so he has to live with them.

Prior to determining stability with a Bode plot, we take the log of Equation 8–18, and plot the logs (Equations 8–19 and 8–20) in Figure 8–6.

$$20 \text{ LOG } |A\beta| = 20 \text{ LOG } |Z| - 20 \text{ LOG } \left|Z_F\left(1 + \frac{Z_B}{Z_F \| Z_B}\right)\right| \tag{8–19}$$

$$\phi = \text{TANGENT}^{-1}(A\beta) \tag{8–20}$$

This enables the designer to add and subtract components of the stability equation graphically.

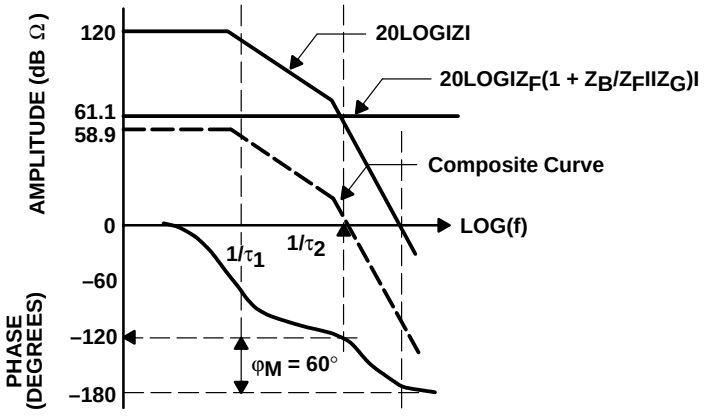

Figure 8–6. Bode Plot of Stability Equation

The plot in Figure 8–6 assumes typical values for the parameters:

$$Z = \frac{1M\Omega}{(1 + \tau_1 S)(1 + \tau_2 S)} \tag{8–21}$$

$$Z_B = 70\Omega \tag{8–22}$$

$$Z_G = Z_F = 1k\Omega \tag{8–23}$$

The transimpedance has two poles and the plot shows that the op amp will be unstable without the addition of external components because 20 LOG|Z| crosses the 0-dB axis after the phase shift is 180°. Z_F, Z_B, and Z_G reduce the loop gain 61.1 dB, so the circuit is stable because it has 60°-phase margin. Z_F is the component that stabilizes the circuit. The parallel combination of Z_F and Z_G contribute little to the phase margin because Z_B is very small, so Z_B and Z_G have little effect on stability.

The manufacturer determines the optimum value of R_F during the characterization of the IC. Referring to Figure 8–6, it is seen that when R_F exceeds the optimum value recommended by the IC manufacturer, stability increases. The increased stability has a price called decreased bandwidth. Conversely, when R_F is less than the optimum value recommended by the IC manufacturer, stability decreases, and the circuit response to step inputs is overshoot or possibly ringing. Sometimes the overshoot associated with less than optimum R_F is tolerated because the bandwidth increases as R_F decreases. The peaked response associated with less than optimum values of R_F can be used to compensate for cable droop caused by cable capacitance.

When $Z_B = 0\ \Omega$ and $Z_F = R_F$ the loop gain equation is; $A\beta = Z/R_F$. Under these conditions Z and R_F determine stability, and a value of R_F can always be found to stabilize the circuit. The transimpedance and feedback resistor have a major impact on stability, and the input buffer's output impedance has a minor effect on stability. Since Z_B increases with an increase in frequency, it tends to increase stability at higher frequencies. Equation 8–18 is rewritten as Equation 8–24, but it has been manipulated so that the ideal closed-loop gain is readily apparent.

$$A\beta = \frac{Z}{Z_F + Z_B\left(1 + \frac{R_F}{R_G}\right)} \tag{8–24}$$

The closed-loop ideal gain equation (inverting and noninverting) shows up in the denominator of Equation 8–24, so the closed-loop gain influences the stability of the op amp. When Z_B approaches zero, the closed-loop gain term also approaches zero, and the op amp becomes independent of the ideal closed-loop gain. Under these conditions R_F determines stability, and the bandwidth is independent of the closed-loop gain. Many people claim that the CFA bandwidth is independent of the gain, and that claim's validity is dependent on the ratios Z_B/Z_F being very low.

Z_B is important enough to warrant further investigation, so the equation for Z_B is given below.

$$Z_B \cong h_{ib} + \frac{R_B}{\beta_0 + 1}\left(\frac{1 + \frac{s\beta_0}{\omega_T}}{1 + \frac{S\beta_0}{(\beta_0+1)\omega_T}}\right) \quad (8\text{–}25)$$

At low frequencies $h_{ib} = 50\ \Omega$ and $R_B/(\beta_0+1) = 25\ \Omega$, so $Z_B = 75\ \Omega$. Z_B varies in accordance with Equation 8–25 at high frequencies. Also, the transistor parameters in Equation 8–25 vary with transistor type; they are different for NPN and PNP transistors. Because Z_B is dependent on the output transistors being used, and this is a function of the quadrant the output signal is in, Z_B has an extremely wide variation. Z_B is a small factor in the equation, but it adds a lot of variability to the current-feedback op amp.

8.7 Selection of the Feedback Resistor

The feedback resistor determines stability, and it affects closed-loop bandwidth, so it must be selected very carefully. Most CFA IC manufacturers employ applications and product engineers who spend a great deal of time and effort selecting R_F. They measure each noninverting gain with several different feedback resistors to gather data. Then they pick a compromise value of R_F that yields stable operation with acceptable peaking, and that value of R_F is recommended on the data sheet for that specific gain. This procedure is repeated for several different gains in anticipation of the various gains their customer applications require (often G = 1, 2, or 5). When the value of R_F or the gain is changed from the values recommended on the data sheet, bandwidth and/or stability is affected.

When the circuit designer must select a different R_F value from that recommended on the data sheet he gets into stability or low bandwidth problems. Lowering R_F decreases stability, and increasing R_F decreases bandwidth. What happens when the designer needs to operate at a gain not specified on the data sheet? The designer must select a new value of R_F for the new gain, but there is no guarantee that new value of R_F is an optimum value. One solution to the R_F selection problem is to assume that the loop gain, $A\beta$, is a linear function. Then the assumption can be made that $(A\beta)_1$ for a gain of one equals $(A\beta)_N$ for a gain of N, and that this is a linear relationship between stability and gain. Equations 8–26 and 8–27 are based on the linearity assumption.

$$\frac{Z}{Z_{F1} + Z_B\left(1 + \frac{Z_{F1}}{Z_{G1}}\right)} = \frac{Z}{Z_{FN} + Z_B\left(1 + \frac{Z_{FN}}{Z_{GN}}\right)} \quad (8\text{–}26)$$

$$Z_{FN} = Z_{F1} + Z_B\left(\left(1 + \frac{Z_{F1}}{Z_{G1}}\right) - \left(1 + \frac{Z_{FN}}{Z_{GN}}\right)\right) \quad (8\text{–}27)$$

Equation 8–27 leads one to believe that a new value for Z_F can easily be chosen for each new gain. This is not the case in the real world; the assumptions don't hold up well enough to rely on them. When you change to a new gain not specified on the data sheet, Equation 8–27, at best, supplies a starting point for R_F, but you must test to determine the final value of R_F.

When the R_F value recommended on the data sheet can't be used, an alternate method of selecting a starting value for R_F is to use graphical techniques. The graph shown in Figure 8–7 is a plot of the typical 300-MHz CFA data given in Table 8–1.

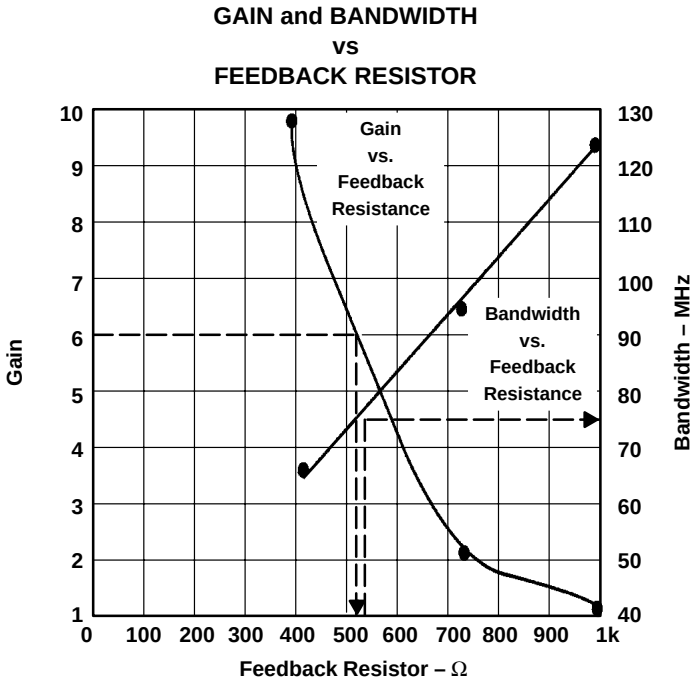

Figure 8–7. Plot of CFA R_F, G, and BW

Table 8–1. Data Set for Curves in Figure 8–7

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
+ 1	1000	125
+ 2	681	95
+ 10	383	65

Enter the graph at the new gain, say A_{CL} = 6, and move horizontally until you reach the intersection of the gain versus feedback resistance curve. Then drop vertically to the resistance axis and read the new value of R_F (500 Ω in this example). Enter the graph at the new value of R_F, and travel vertically until you intersect the bandwidth versus feedback resistance curve. Now move to the bandwidth axis to read the new bandwidth (75 MHz in this example). As a starting point you should expect to get approximately 75 MHz BW with a gain of 6 and R_F = 500 Ω. Although this technique yields more reliable solutions than Equation 8–27 does, op amp peculiarities, circuit board stray capacitances, and wiring make extensive testing mandatory. The circuit must be tested for performance and stability at each new operating point.

8.8 Stability and Input Capacitance

When designer lets the circuit board introduce stray capacitance on the inverting input node to ground, it causes the impedance Z_G to become reactive. The new impedance, Z_G, is given in Equation 8–28, and Equation 8–29 is the stability equation that describes the situation.

$$Z_G = \frac{R_G}{1 + R_G C_G s} \tag{8–28}$$

$$A\beta = \frac{Z}{Z_B + \dfrac{Z_F}{Z_G^2 + Z_B Z_G}} \tag{8–29}$$

$$A\beta = \frac{Z}{R_F\left(1 + \dfrac{R_B}{R_F \| R_G}\right)\left(1 + R_B \parallel R_F \parallel R_G C_G s\right)} \tag{8–30}$$

Equation 8–29 is the stability equation when Z_G consists of a resistor in parallel with stray capacitance between the inverting input node and ground. The stray capacitance, C_G, is a fixed value because it is dependent on the circuit layout. The pole created by the stray capacitance is dependent on R_B because it dominates R_F and R_G. R_B fluctuates with manufacturing tolerances, so the $R_B C_G$ pole placement is subject to IC manufacturing tolerances. As the $R_B C_G$ combination becomes larger, the pole moves towards the zero fre-

quency axis, lowering the circuit stability. Eventually it interacts with the pole contained in Z, $1/\tau_2$, and instability results.

The effects of stray capacitance on CFA closed-loop performance are shown in Figure 8–8.

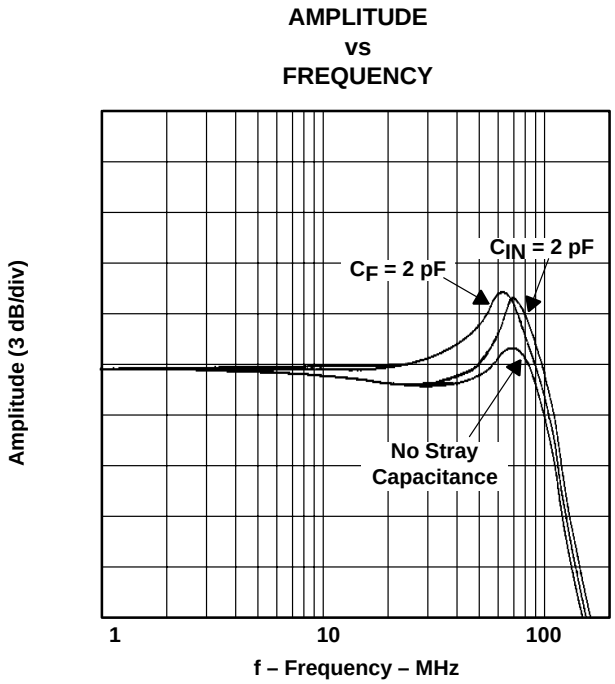

Figure 8–8. Effects of Stray Capacitance on CFAs

Notice that the introduction of C_G causes more than 3 dB peaking in the CFA frequency response plot, and it increases the bandwidth about 18 MHz. Two picofarads are not a lot of capacitance because a sloppy layout can easily add 4 or more picofarads to the circuit.

8.9 Stability and Feedback Capacitance

When a stray capacitor is formed across the feedback resistor, the feedback impedance is given by Equation 8–31. Equation 8–32 gives the loop gain when a feedback capacitor has been added to the circuit.

$$Z_F = \frac{R_F}{1 + R_F C_F s} \tag{8–31}$$

$$A\beta = \frac{Z\left(1 + R_F C_F s\right)}{R_F\left(1 + \frac{R_B}{R_F \| R_G}\right)\left(1 + R_B \| R_F \| R_G C_F s\right)} \tag{8–32}$$

This loop gain transfer function contains a pole and zero, thus, depending on the pole/zero placement, oscillation can result. The Bode plot for this case is shown in Figure 8–9. The original and composite curves cross the 0-dB axis with a slope of –40 dB/decade, so either curve can indicate instability. The composite curve crosses the 0-dB axis at a higher frequency than the original curve, hence the stray capacitance has added more phase shift to the system. The composite curve is surely less stable than the original curve. Adding capacitance to the inverting input node or across the feedback resistor usually results in instability. R_B largely influences the location of the pole introduced by C_F, thus here is another case where stray capacitance leads to instability.

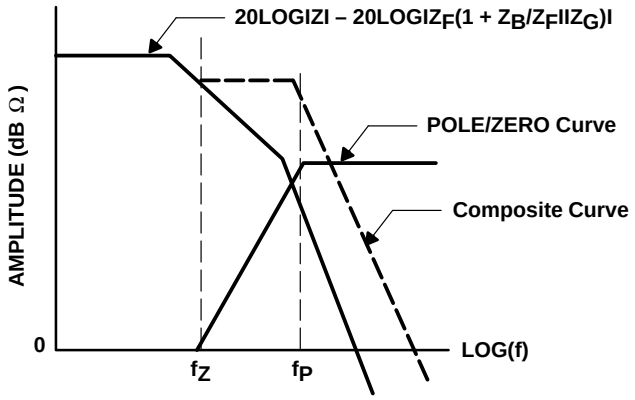

Figure 8–9. Bode Plot with C_F

Figure 8–8 shows that C_F = 2 pF adds about 4 dB of peaking to the frequency response plot. The bandwidth increases about 10 MHz because of the peaking. C_F and C_G are the major causes of overshoot, ringing, and oscillation in CFAs, and the circuit board layout must be carefully done to eliminate these stray capacitances.

8.10 Compensation of C_F and C_G

When C_F and C_G both are present in the circuit they may be adjusted to cancel each other out. The stability equation for a circuit with C_F and C_G is Equation 8–33.

$$A\beta = \frac{Z\left(1 + R_F C_F s\right)}{R_F\left(1 + \dfrac{R_B}{R_F \| R_G}\right)\left(R_B \| R_F \| R_G \left(C_F + C_G\right) s + 1\right)} \tag{8–33}$$

If the zero and pole in Equation 8–33 are made to cancel each other, the only poles remaining are in Z. Setting the pole and zero in Equation 8–33 equal yields Equation 8–34 after some algebraic manipulation.

$$R_F C_F = C_G\left(R_G \| R_B\right) \tag{8–34}$$

R_B dominates the parallel combination of R_B and R_G, so Equation 8–34 is reduced to Equation 8–35.

$$R_F C_F = R_B C_G \tag{8–35}$$

R_B is an IC parameter, so it is dependent on the IC process. R_B it is an important IC parameter, but it is not important enough to be monitored as a control variable during the manufacturing process. R_B has widely spread, unspecified parameters, thus depending on R_B for compensation is risky. Rather, the prudent design engineer assures that the circuit will be stable for any reasonable value of R_B, and that the resulting frequency response peaking is acceptable.

8.11 Summary

Constant gain-bandwidth is not a limiting criterion for the CFA, so the feedback resistor is adjusted for maximum performance. Stability is dependent on the feedback resistor; as R_F is decreased, stability is decreased, and when R_F goes to zero the circuit becomes unstable. As R_F is increased stability increases, but the bandwidth decreases.

The inverting input impedance is very high, but the noninverting input impedance is very low. This situation precludes CFAs from operation in the differential amplifier configuration. Stray capacitance on the inverting input node or across the feedback resistor always leads to peaking, usually to ringing, and sometimes to oscillations. A prudent circuit designer scans the PC board layout for stray capacitances, and he eliminates them. Breadboarding and lab testing are a must with CFAs. The CFA performance can be improved immeasurably with a good layout, good decoupling capacitors, and low inductance components.

Chapter 9

Voltage- and Current-Feedback Op Amp Comparison

Ron Mancini and James Karki

9.1 Introduction

The name, operational amplifier, was given to voltage-feedback amplifiers (VFA) when they were the only op amps in existence. These new (they were new in the late '40s) amplifiers could be programmed with external components to perform various math operations on a signal; thus, they were nicknamed op amps. Current-feedback amplifiers (CFA) have been around approximately twenty years, but their popularity has only increased in the last several years. Two factors limiting the popularity of CFAs is their application difficulty and lack of precision.

The VFA is familiar component, and there are several variations of internally compensated VFAs that can be used with little applications work. Because of its long history, the VFA comes in many varieties and packages, so there are VFAs applicable to almost any job. VFA bandwidth is limited, so it can't function as well at high signal frequencies as the CFA can. For now, the signal frequency and precision separates the applications of the two op amp configurations.

The VFA has some other redeeming virtues, such as excellent precision, that makes it the desirable amplifier in low frequency applications. Many functions other than signal amplification are accomplished at low frequencies, and functions like level-shifting a signal require precision. Fortunately, precision is not required in most high frequency applications where amplification or filtering of a signal is predominant, so CFAs are suitable to high frequency applications. The lack of precision coupled with the application difficulties prevents the CFA from replacing the VFA.

9.2 Precision

The long-tailed pair input structure gives the VFA its precision; the long-tailed pair is shown in Figure 9–1

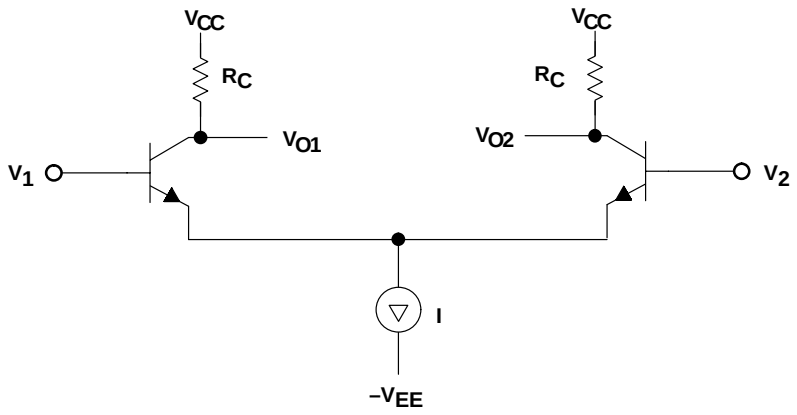

Figure 9–1. Long-Tailed Pair

The transistors, Q_1 and Q_2, are very carefully matched for initial and drift tolerances. Careful attention is paid to detail in the transistor design to insure that parameters like current gain, β, and base-emitter voltage, V_{BE}, are matched between the input transistors, Q_1 and Q_2. When $V_{B1} = V_{B2}$, the current, I, splits equally between the transistors, and $V_{O1} = V_{O2}$. As long as the transistor parameters are matched, the collector currents stay equal. The slightest change of V_{B1} with respect to V_{B2} causes a mismatch in the collector currents and a differential output voltage $|V_{B1}–V_{B2}|$.

When temperature or other outside influences change transistor parameters like current gain or base-emitter voltage, as long as the change is equal, it causes no change in the differential output voltage. IC designers go to great lengths to ensure that transistor parameter changes due to external influences do not cause a differential output voltage change. Now, the slightest change in either base voltage causes a differential output voltage change, and gross changes in external conditions do not cause a differential output voltage change. This is the formula for a precision amplifier because it can amplify small input changes while ignoring changes in the parameters or ambient conditions.

This is a simplified explanation, and there are many different techniques used to ensure transistor matching. Some of the techniques used to match input transistors are parameter trimming, special layout techniques, thermal balancing, and symmetrical layouts. The long-tailed pair is an excellent circuit configuration for obtaining precision in the input circuit, but the output circuit has one fault. The output circuit collector impedance has to be high to achieve high gain in the first stage. High impedance coupled with the Miller capacitance discussed in Chapter 7 forms a quasidominant pole compensation circuit that has poor high frequency response.

The noninverting input of the CFA (see Figure 9–2) connects to a buffer input inside the op amp. The inverting input of the CFA connects to a buffer output inside the CFA. Buffer inputs and outputs have dramatically different impedance levels, so any matching becomes a moot point. The buffer can't reject common-mode voltages introduced by parameter drifts because it has no common-mode rejection capability. The input current causes a voltage drop across the input buffer's output impedance, R_B, and there is no way that this voltage drop can be distinguished from an input signal.

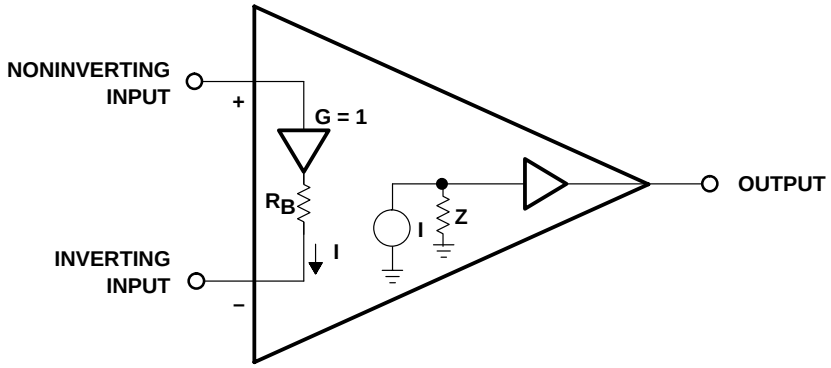

Figure 9–2. Ideal CFA

The CFA circuit configuration was selected for high frequency amplification because it has current-controlled gain and a current-dominant input. Being a current device, the CFA does not have the Miller-effect problem that the VFA has. The input structure of the CFA sacrifices precision for bandwidth, but CFAs achieve usable bandwidths ten times the usable VFA bandwidth.

9.3 Bandwidth

The bandwidth of a circuit is defined by high frequency errors. When the gain falls off at high frequencies unequal frequency amplification causes the signal to become distorted. The signal loses its high frequency components; an example of high frequency signal degradation is a square wave with sharp corners that is amplified and turned into slump cornered semi sine wave. The error equation for any feedback circuit is repeated in Equation 9–1.

$$E = \frac{V_{IN}}{1 + A\beta} \tag{9–1}$$

This equation is valid for any feedback circuit, so it applies equally to a VFA or a CFA. The loop gain equation for any VFA is repeated as Equation 9–2.

$$A\beta = \frac{aR_G}{R_F + R_G} \tag{9–2}$$

Equation 9–2 is rewritten below as Equations 9–3 and 9–4 for the noninverting and inverting circuits respectively. In each case, the symbol G_{CLNI} and G_{CLI} represent the closed loop gain for the noninverting and inverting circuits respectively.

$$A\beta = \frac{a}{\frac{R_F + R_G}{R_G}} = \frac{a}{G_{CLNI}} \tag{9–3}$$

$$A\beta = \frac{a}{\frac{R_F + R_G}{R_G}} = \frac{a}{G_{CLI} + 1} \tag{9–4}$$

In both cases the loop gain decreases as the closed loop gain increases, thus all VFA errors increase as the closed loop gain increases. The error increase is mathematically coupled to the closed loop gain equation, so there is no working around this fact. For the VFA, effective bandwidth decreases as the closed loop gain increases because the loop gain decreases as the closed loop gain increases.

A plot of the VFA loop gain, closed loop gain, and error is given in Figure 9–3. Referring to Figure 9–3, the direct gain, A, is the op amp open loop gain, a, for a noninverting op amp. The direct gain for an inverting op amp is $(a(Z_F/(Z_G + Z_F)))$. The Miller effect causes the direct gain to fall off at high frequencies, thus error increases as frequency increases because the effective loop gain decreases. At a given frequency, the error also increases when the closed loop gain is increased.

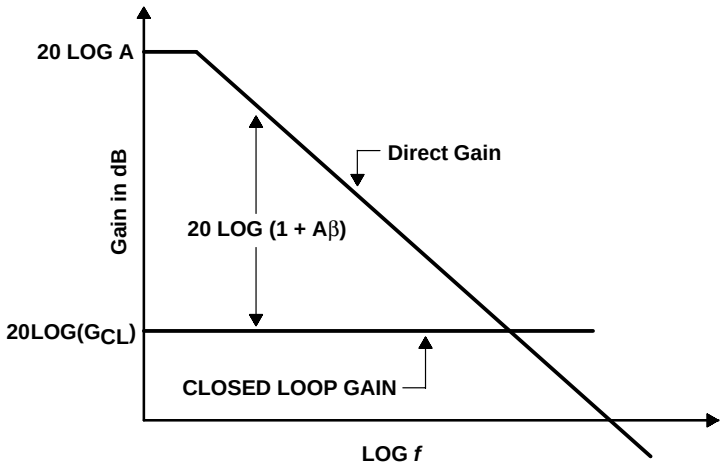

Figure 9–3. VFA Gain versus Frequency

The CFA is a current operated device; hence, it not nearly as subject to the Miller effect resulting from stray capacitance as the VFA is. The absence of the Miller effect enables the CFA's frequency response to hold up far better than the VFA's does. A plot of the CFA loop gain, transimpedance, and error is given in Figure 9–4. Notice that the transimpedance stays at the large low frequency intercept value until much higher frequencies than the VFA does.

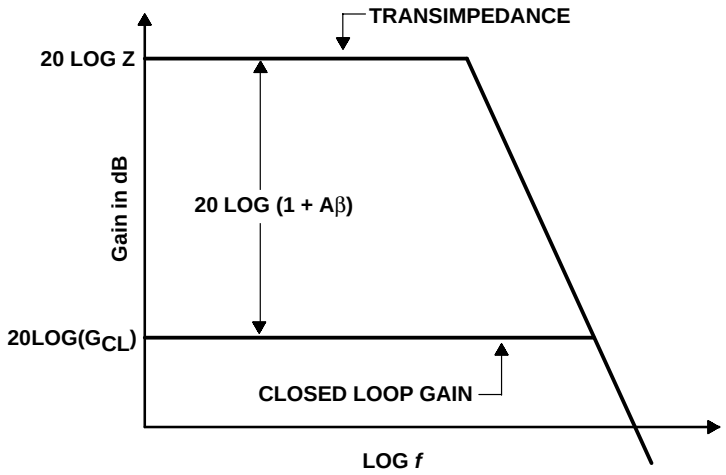

Figure 9–4. CFA Gain vs Frequency

The loop gain equation for the CFA is repeated here as Equation 9–5.

$$A\beta = \frac{Z}{R_F\left(1 + \frac{R_B}{R_F \| R_G}\right)} \tag{9–5}$$

When the input buffer output resistance approaches zero, Equation 9–5 reduces to Equation 9–6.

$$A\beta = \frac{Z}{R_F} \tag{9–6}$$

Equation 9–6 shows that the closed-loop gain has no effect on the loop gain when R_B = 0, so under ideal conditions one would expect the transimpedance to fall off with a zero slope. Figure 9–4 shows that there is a finite slope, but much less than that of a VFA, and the slope is caused by R_B not being equal to zero. For example, R_B is usually 50 Ω when R_F = 1000 Ω at A_{CL} = 1. If we let $R_F = R_G$, then $R_F \| R_G$ = 500 Ω, and $R_B/R_F \| R_G$ = 50/500 = 0.1.

Substituting this value into Equation 9–6 yields Equation 9–7, and Equation 9–7 is almost identical to Equation 9–6. R_B does cause some interaction between the loop gain and the transimpedance, but because the interaction is secondary the CFA gain falls off with a faster slope.

$$A\beta = \frac{Z}{1.1\ R_F} \tag{9–7}$$

The direct gain of a VFA starts falling off early, often at 10 Hz or 100 Hz, but the transimpedance of a CFA does not start falling off until much higher frequencies. The VFA is constrained by the gain-bandwidth limitation imposed by the closed loop gain being incorporated within the loop gain. The CFA, with the exception of the effects of R_B, does not have this constraint. This adds up to the CFA being the superior high frequency amplifier.

9.4 Stability

Stability in a feedback system is defined by the loop gain, and no other factor, including the inputs or type of inputs, affects stability. The loop gain for a VFA is given in Equation 9–2. Examining Equation 9–2 we see that the stability of a VFA is depends on two items; the op amp transfer function, a, and the gain setting components, Z_F/Z_G.

The op amp contains many poles, and if it is not internally compensated, it requires external compensation. The op amp always has at least one dominant pole, and the most phase margin that an op amp has is 45°. Phase margins beyond 60° are a waste of op amp bandwidth. When poles and zeros are contained in Z_F and Z_G, they can compensate for the op amp phase shift or add to its instability. In any case, the gain setting components always affect stability. When the closed-loop gain is high, the loop gain is low, and low loop gain circuits are more stable than high loop gain circuits.

Wiring the op amp to a printed circuit board always introduces components formed from stray capacitance and inductance. Stray inductance becomes dominant at very high frequencies, hence, in VFAs, it does not interfere with stability as much as it does with signal handling properties. Stray capacitance causes stability to increase or decrease depending on its location. Stray capacitance from the input or output lead to ground induces instability, while the same stray capacitance in parallel with the feedback resistor increases stability.

The loop gain for a CFA with no input buffer output impedance, R_B, is given in Equation 9–6. Examining Equation 9–6 we see that the stability of a CFA depends on two items: the op amp transfer function, Z, and the gain setting component, Z_F. The op amp contains many poles, thus they require external compensation. Fortunately, the external compensation for a CFA is done with Z_F. The factory applications engineer does extensive testing to determine the optimum value of R_F for a given gain. This value should be used in all applications at that gain, but increased stability and less peaking can be obtained by increasing R_F. Essentially this is sacrificing bandwidth for lower frequency performance, but in applications not requiring the full bandwidth, it is a wise tradeoff.

The CFA stability is not constrained by the closed-loop gain, thus a stable operating point can be found for any gain, and the CFA is not limited by the gain-bandwidth constraint. If the optimum feedback resistor value is not given for a specific gain, one must test to find the optimum feedback resistor value.

Stray capacitance from any node to ground adversely affects the CFA performance. Stray capacitance of just a couple of pico Farads from any node to ground causes 3 dB or more of peaking in the frequency response. Stray capacitance across the CFA feedback resistor, quite unlike that across the VFA feedback resistor, always causes some form of instability. CFAs are applied at very high frequencies, so the printed circuit board inductance associated with the trace length and pins adds another variable to the stability equation. Inductance cancels out capacitance at some frequency, but this usually seems to happen in an adverse manner. The wiring of VFAs is critical, but the wiring of CFAs is a science. Stay with the layout recommended by the manufacturer whenever possible.

9.5 Impedance

The input impedance of a VFA and CFA differ dramatically because their circuit configurations are very different. The VFA input circuit is a long-tailed pair, and this configuration gives the advantages that both input impedances match. Also, the input signal looks into an emitter-follower circuit that has high input impedance. The emitter-follower input impedance is $\beta(r_e + R_E)$ where R_E is a discrete emitter resistor. At low input currents, R_E is very high and the input impedance is very high. If a higher input impedance is required, the op amp uses a Darlington circuit that has an input impedance of $\beta^2(r_e + R_E)$.

So far, the implicit assumption is that the VFA is made with a bipolar semiconductor process. Applications requiring very high input impedances often use a FET process. Both BIFET and CMOS processes offer very high input impedance in any long-tailed pair configuration. It is easy to get matched and high input impedances at the amplifier inputs. Do not confuse the matched input impedance at the op amp leads with the overall circuit input impedance. The input impedance looking into the inverting input is R_G, and the impedance looking into the noninverting input is the input impedance of the op amp. While these are two different impedances, they are mismatched because of the circuit not the op amp.

The CFA has a radically different input structure that causes it to have mismatched input impedances. The noninverting input lead of the CFA is the input of a buffer that has very high input impedance. The inverting input lead is the output of a buffer that has very low impedance. There is no possibility that these two input impedances can be matched.

Again, because of the circuit, the inverting circuit input impedance is R_G. Once the circuit gain is fixed, the only way to increase R_G is to increase R_F. But, R_F is determined by a tradeoff between stability and bandwidth. The circuit gain and bandwidth requirements fix R_F, hence there is no room to further adjust R_F to raise the resistance of R_G. If the manufacturer's data sheet says that $R_F = 100\ \Omega$ when the closed-loop gain is two, then

R_G = 100 Ω or 50 Ω depending on the circuit configuration. This sets the circuit input impedance at 100 Ω. This analysis is not entirely accurate because R_B adds to the input impedance, but this addition is very small and dependent on IC parameters. CFA op amp circuits are usually limited to noninverting voltage applications, but they serve very well in inverting applications that are current-driven.

The CFA is limited to the bipolar process because that process offers the highest speed. The option of changing process to BIFET or CMOS to gain increased input impedance is not attractive today. Although this seems like a limiting factor, it is not because CFAs are often used in low impedance where the inputs are terminated in 50 Ω or 75 Ω. Also, most very high-speed applications require low impedances.

9.6 Equation Comparison

The pertinent VFA and CFA equations are repeated in Table 9–1. Notice that the ideal closed-loop gain equations for the inverting and noninverting circuits are identical. The ideal equations for the VFA depend on the op amp gain, a, being very large thus making Aβ large compared to one. The CFA needs two assumptions to be valid to obtain the ideal equations. First, the ideal equations for the CFA depend on the op amp transimpedance, Z, being very large thus making Aβ large compared to one. Second, R_B must be very small compared to $Z_F||Z_G$.

The ideal gain equations are identical, but the applications are very different because the VFA is best applied to lower frequency precision jobs while the CFA applications are in the very high frequency realm. The transimpedance in a CFA acts much like the gain does in a VFA. In each case, transimpedance or gain, it is the parameter that enables the use of feedback.

Table 9–1. Tabulation of Pertinent VFA and CFA Equations

CIRCUIT CONFIGURATION	CURRENT FEEDBACK AMPLIFIER	VOLTAGE FEEDBACK AMPLIFIER
NONINVERTING		
Forward or direct gain	$\frac{Z\left(1 + Z_F/Z_G\right)}{Z_F\left(1 + Z_B/Z_F \parallel Z_G\right)}$	a
Actual closed loop gain	$\frac{Z_F\left(1+\frac{Z_B}{Z_G}\right)}{Z_F\left(1+\frac{Z_B}{Z_F \parallel Z_G}\right)}{1 + \frac{Z}{Z_F\left[1+\frac{Z_B}{\frac{1+Z_B}{Z_F \parallel Z_G}}\right]}}$	$\frac{a}{1 + \frac{aZ_G}{Z_F \parallel Z_G}}$
Closed loop gain	$1 + Z_F/Z_G$	$1 + Z_F/Z_G$
INVERTING		
Forward or direct gain	$\frac{Z}{Z_G\left(1 + Z_B/Z_F \parallel Z_G\right)}$	$aZ_F/\left(Z_F + Z_G\right)$
Ideal loop gain	$Z/Z_F\left(1 + Z_B/Z_F \parallel Z_G\right)$	$aZ_G/\left(Z_G + Z_F\right)$
Actual closed loop gain	$\frac{-Z_G\left(1 + \frac{Z_B}{Z_F \parallel Z_G}\right)}{1 + \frac{Z}{Z_F\left(1+\frac{Z_B}{Z_F \parallel Z_G}\right)}}$	$\frac{\frac{-aZ_F}{Z_F+Z_G}}{1 + \frac{aZ_G}{Z_F \parallel Z_G}}$
Closed loop gain	$-Z_F/Z_G$	$-Z_F/Z_G$

A

B

C

D

E

F

G

H

I

K

L

M

N

O

P

Q

R

S

T

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W